Non-unit protection of series compensated transmission lines using high frequency fault signals

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NON-UNIT PROTECTION OF SERIES COMPENSATED TRANSMISSION LINES USING HIGH FREQUENCY FAULT SIGNALS

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ABSTRACT

Series capacitors offer considerable technical and economic advantages in long distance AC transmission. In particular, their excellent reliability and minimal maintenance requirements make series compensation the most cost effective method of enhancing the power transfer capability of an interconnection. Extra high voltage (EHV) lines employing series capacitors, however, pose difficult problem for the conventional line protection relays, particularly those that are based on nonunit principles. For example, the complex variation of line impedance is accentuated as the capacitors's own protection equipment operates randomly under fault conditions; this can cause a serious degradation in the performance of impedance measuring devices such as distance protection.

This thesis describes a new protection technique for accurately detecting faults on series compensated line using fault generated high frequency (HF) voltage signals. The technique involves the use of conventionally connected power line carrier line traps and capacitor voltage transformers (CVTs). Fault generated HF voltage signals are captured by means of a stack-tuner circuit which is connected to a transmission line via the high voltage coupling capacitor of a typical CVT. A very high sampling rate is used to capture these signals which are then processed using digital signal

processing techniques. Power line carrier line traps are used to confine the HF signals to the protected zone and their bandstop characteristics are used as a basis for discriminating between internal and external faults. It is a non-unit technique as it only uses locally derived information but it has the discriminative properties normally associated with unit protection schemes.

The relay performance is demonstrated by digitally simulating a variety of internal and external faults on different 500 kV series compensated networks employing different types of capacitor protective schemes including those employing non-linear resistors. These show that the technique is capable of discriminating between internal and external faults in less than approximately five milliseconds. It is not adversely affected by factors such as fault type, position or inception angle. More importantly, the new relay scheme has been developed to satisfactorily deal with the longstanding protection problems associated with series compensated lines.

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LIST OF ABBREVIATIONS AND SYMBOLS

a_{nk}, b_{nk}	Digital filter coefficients
AC	Alternating Current
ACSR	Aluminium Conductor Steel Reinforced
A/D	Analogue to Digital
B1	By-pass breaker
B2	Reinsertion breaker
C	Digital filter gain
C	Capacitor bank
C_1, C_2, L_1, L_2, R_1	Line trap parameters
C_c	Coupling capacitor
C_p, L_p, R_p	Stack tuner parameters
C_s	Busbar stray shunt capacitance
CAD	Computer Aided Design
CB	Circuit Breaker
CT	Current Transformer
CVT	Capacitor Voltage Transformer
C(n)	Counter value
d	Discrimination ratio
D	Damping circuit

DGS	Dual Gap Scheme
DGNS	Dual Gap / Non-linear resistor Scheme
DQL	Digital Quantum Levels
EHV	Extra High Voltage
EMTP	Electro-Magnetic Transients Program
F_n	Fault positions
FACTS	Flexible AC Transmission Systems
g	Time varying arc conductance
G	Triggered air gap
G	Stationary arc conductance
G1	Spark gap high set
G2	Spark gap low set
GVA	Giga Volt Amperes
HF	High Frequency
HV	High Voltage
Hz	Hertz
$H(S)$	Anti-aliasing filter transfer function
$H(Z)$	Digital filter transfer function
i	Arc current
$\boldsymbol{I}$	Phase current vector
$\boldsymbol{I}^c$	Model current vector
I_{fl}	Full load current
I_0	Zero sequence current
IIR	Infinite Impulse Response

k	Summation variable
kHz	Kilo-Hertz
kV	Kilo-Volts
l	Time dependant arc length
L	Moving average filter length
L_s	CVT inductance
LT	Line trap
ms	Milli-second(s)
MHz	Mega-Hertz
MOV	Metal-Oxide Varistor
n	Time step number
NR	Non-linear resistor
NGC	National Grid Company
$\mathbf{P}$	Square matrix whose Eigenvectors are the Modal constants
P_L	Power transfer capability of a transmission line
P_m	Mean power
PLC	Power Line Carrier
$\mathbf{Q}$	Modal current matrix
rms	Root mean square value
R	Resistive component per unit arc length
$\mathbf{R_s}$	Source resistance
sec	Second(s)
S	Laplace domain operator
$\mathbf{S}$	Modal voltage matrix

ST	Stack tuner
SVA	Source short circuit level
t	Time
Δt	Sampling interval
T	Period of a continuous time signal
T_f	Fault inception time
T_g	Capacitor gap flashover time
TP	Trip Level
TACS	Transient Analysis of Control Systems
UHS	Ultra High Speed
V	Phase voltage vector
V_a, V_b, V_c	Phase voltages
V_R	Receiving end voltage
V_S	Sending end voltage
V_X, V_Y	Modal voltages
V_o	Constant voltage parameter per unit arc length
V^c	Modal voltage vector
V_f	Bandpass filter output
V_L	Operating line voltage
$Vz(n\Delta t)$	Enhanced filter output
VT	Voltage Transformer
w_p	Small window length defined in the auxiliary scheme logic
$x(t)$	Time domain signal
X_{cap}	Capacitive reactance

X_L	Inductive reactance of the transmission line
X_m	Mutual impedance
$\mathbf{X_s}$	Source reactance
X:R	Source impedance ratio
$\mathbf{Y}$	Line admittance matrix
Z	Z domain operator
$\mathbf{Z}$	Line impedance matrix
Z_1	Positive phase sequence impedance
Z_2	Negative phase sequence impedance
Z_0	Zero sequence phase impedance
Z_L	Distance relay impedance setting without series compensation
Z_L'	Distance relay impedance setting with series compensation
Z_n	Neural impedance
$\mathbf{Z_s}$	Source impedance
Z_{se}	Self impedance
Z_{so}: Z_{s1}	Source zero phase sequence to positive phase sequence impedance
δ	Phase angle between sending end voltage and receiving end voltage
θ	Line impedance angle
τ	Arc time constant
μF	Micro-farads(s)
μs	Micro-second(s)

CHAPTER 1

INTRODUCTION

The history of electrical-power technology throughout the world is one of steady and, in recent years, rapid progress, which has made it possible to design and construct economic and reliable power systems capable of satisfying the continuing growth in the demand for electrical energy. In this respect, power system protection and control play a significant part, and progress in the design and development in these fields is a vital prerequisite for the efficient operation and continuing development of power supply systems as a whole.

1.1 Basic Structure of Electric Power Systems

The structure of the electric power system is very large and complex. Electrical energy is generated in large hydro-electric, thermal and nuclear power stations. These stations are generally situated far away from the load centres. This necessitates an

extensive power supply network between the generating stations and the consumers' loads. This network may be divided into three parts, viz., transmission system, subtransmission system and distribution system. In general, the generation and transmission systems are referred to as *bulk power supply*, and the subtransmission and distribution systems are considered to be the final means to transfer the electric energy to the individual consumers. Bulk power transmission is made of a high-voltage network, generally 115 - 750 kV alternating current, designed to interconnect power plants and electrical utility systems and to transmit power from the generating plants to major load centres.

1.1.1 Long line AC Transmission

Transmission lines are the connecting links between the generating stations and the distribution systems and lead to the other power systems over interconnections. In order to transmit the necessary power over long distances, line losses become increasingly important. However, the losses encountered when transmitting electricity are associated with the ohmic heating of the conductors and so they can be minimised by keeping the current flow as low as possible. To maintain the ability to transmit the necessary power, the voltage must be raised. Roughly, the transmission capability of lines of the same length varies at a rate somewhat greater than the square of the voltage. Generator voltage is stepped up to transmission levels; in the United Kingdom, this is at 275 kV and 400 kV, whilst many overseas countries have transmission systems operating at 500 kV and 750 kV.

A transmission system comprising of short lines is fairly stiff at the generator ends (busbars) because there are a number of infeeding lines from other sources connected to the busbar. As the line is short, both the line reactance and capacitance are relatively small, and in fact the latter can be neglected. This means that a generator can operate at a reasonably low load angle in order to transmit an appreciable amount of power over the line, thus minimising the problem of generator instability due to disturbances. Because of the stiffness of busbars and the interconnection of the system, even when a line does go out due to a fault, the majority of faults being transitory in nature anyway, a three-phase autoreclosure scheme is successfully employed without loss of stability or any serious disruption.

However, on long lines where the source of generation is often remote from the load points, (especially in countries which employ hydro-power schemes and also where the system is not so fully integrated) the system at the generator end is very weak. In fact, in the majority of cases, there are just one or two machines connected to a busbar and the feeder is more of a radial type, ie. the line is single-end fed with a large load at the other end. In such cases, the problem of maintaining stability becomes that much greater. Double circuit lines are very uneconomical to use because of the very long distances involved. Thus, as there is only one single circuit line, three-phase autoreclosure schemes in which all the three phase conductors are isolated for any type of fault, are not very practical, because in the majority of cases the closing of the breakers is not fast enough to maintain stability. Single pole autoreclosure techniques can be used to advantage in such cases.

Because the line is long, both the line inductance and capacitance are large. The increase in line inductance has the following main effects:

1. The power transfer capability of the line is reduced.
2. Both the transient and steady-state stability margins of the system for a given power transfer are lowered.
3. The voltage drop becomes excessive.

The power transfer capability, P_L, of a transmission line is approximately given by equation 1.1 :

$$P_L = \frac{V_S V_R}{X_L} \sin\delta \qquad (1.1)$$

where, V_S and V_R are the sending and receiving end voltages respectively and X_L is the inductive reactance of the transmission circuit between the terminals, and δ is the phase angle between V_S and V_R. The power transfer capability can be increased by either increasing V_S, V_R or δ, or decreasing X_L. The maximum value by which V_S and V_R can be increased to are normally fixed by the steady-state and transient insulation limitations of the transmission system itself. This includes the line and terminal equipment. The value of X_L is determined by the line and terminal equipment (transformers, generators, etc) reactances, the minimum value of which is limited by the physical size of equipment and economic considerations. One of the most effective and economical means of compensating large inductive reactances of the EHV long transmission lines is by incorporating a series capacitor in the line.

1.1.2 Series Compensation

A series capacitor employed in HV networks has evolved into a reliable elements in transmission systems, achieving an excellent performance and reliability standards over a number of years [1,2,3]. By electrically reducing the effective transmission line lengths brought about by the cancellation of part of the inductive reactance, series compensation offers the following major technical advantages over uncompensated systems:

(1) Improvements in the performance of the transmission lines since the steady state power transfer capability of the line becomes proportional to the degree of series compensation. This implies that the same level of power transfer can be achieved for a reduced load angle between the generation voltages at the line ends, thereby offering some improvement in terms of system stability.

(2) The scope for regulating the line voltage as well as reducing the voltage drop along the line.

(3) The possibility of attaining more favourable load distributions between different lines functioning in parallel.

(4) The capacitors are self-regulative since their output voltamperes are directly proportional to the line current flowing through them, thus improving the reactive power balance of the system.

(5) Extremely small losses and good reliability.

(6) Providing a cheaper substitute as an alternative to construction of new lines.

In summary, series capacitor compensation improves the steady-state transmission characteristic of a power network and reduces transmission losses and costs.

1.2 Power System Faults

Power system faults can be caused by a wide variety of reasons such as lightning, ice, heavy winds, trees falling across lines, animals, and humans. Faults can involve any combination of conductors and can be clear of earth as well as being short circuited to earth. The principal fault types are: phase-to-earth (single-phase); phase-to-phase (two phase); double phase-to-earth (phase-phase-earth); and three-phase with and without earth connection. These faults produce over-current and/or over-voltages at various points on the power system, and must be located and cleared before damage is caused to expensive equipments. Electrical faults can occur at any point in a power system and the most exposed parts are overhead transmission lines.

Lightning is the greatest cause of overhead transmission line outages and lightning strikes can affect transmission lines in different ways. The shield wires installed above phase conductors can effectively shield the phase conductors from direct lightning strokes, but if a conductor is struck, the induced overvoltage can cause a flashover across an insulator string. A lightning strike on the ground wire does not always prevent a fault from occurring. A low magnitude surge may be induced which does not cause any problem, or the lighting strike may cause the potential of the nearest tower to rise sufficiently to cause a back flashover from the tower to a phase conductor, initiating a fault. Once an ionised path has been formed, the phase voltage may maintain the fault as the tower potential decays to zero.

Faults caused by equipment failure, human error and foreign objects getting too close

to the power conductors, for example branches of trees, man made items such as cranes, vehicles colliding with towers or poles etc, form generally a high impedance fault path and so only a relatively low fault current flows. These types of faults can be very difficult to detect using conventional methods and so may not be removed from the power system very rapidly.

Most of the faults occurring on power systems are not the balanced three-phase type but the unbalanced, especially the single phase-to-ground type. In general, the three-phase-to-earth and three-phase clear of earth faults are considered to be the most severe. The objectives of power system protection are to detect the presence of faults and to initiate the isolation of the affected equipment in the shortest possible time. However, it is vital that only the faulted item be isolated so that disruption to consumers is minimised.

This thesis presents a new protection technique for accurately detecting faults on series compensated lines; it is based on utilising the fault-induced high frequency voltage signals at any one end of the line.

1.3 The Structure of the Thesis

Chapter 2

A literature search of protection techniques for series compensated EHV transmission lines are presented in this chapter. The line protection problems associated with series

compensated lines have been discussed in detail, particularly with regard to distance protection. Some of the more recent protection techniques are also reviewed in this chapter. Each technique is described individually and some of the advantages and disadvantages are discussed.

Chapter 3

This chapter describes how the high frequency voltage signals are captured and the high voltage equipment that is required to do this. The basic principles of the new protective scheme for the series compensation system are also described in this chapter.

Chapter 4

This chapter describes the simulation of power systems under faults to generate accurate and realistic fault data to develop the protection algorithm and this is achieved through the employment of the well proven Electro-Magnetic Transients Program (EMTP). The primary arc model used is detailed and the modelling of the series compensated EHV transmission lines is described along with the configurations of the power sources and the various types of independent protection equipment associated with the series capacitor banks. In particular, attention is focused upon the modelling of the non-linear Metal-Oxide Varistor elements which form an integral part of the most modern capacitor protection units.

Chapter 5

A complete breakdown of the individual components within the new protection system, as implemented in software, is described in this chapter. The various analogue and digital functions including pre-filtering, modal mixing, signal limiting, analogue to digital conversion, background noise considerations, digital filtering, signal enhancement and the decision processing are all explained.

Chapter 6

A comprehensive relay performance for the systems with MOV capacitor protective scheme is included in this chapter. Some typical results for internal and external faults are presented. The scheme's performance for different fault inception angle, fault types and fault positions is evaluated. Its effectiveness is also examined for high resistance faults, source capacity variations, line loading and degree of series compensation. In addition, relay performance for midpoint series compensated systems and sensitivity to line trap and stack tuner parameter variations are assessed.

Chapter 7

This chapter presents complete relay performance for the systems with conventional capacitor protective schemes. Some typical results for internal and external faults are presented for different system configurations. The various types of capacitor bank protections are included in order to establish any effects that they have on the relay performance, particularly when external faults occur. Finally, relay performance is

evaluated for a more complex and realistic power system network and investigates how the new relay overcome and deal with protection problems encountered on the series compensated lines under practical situations.

Chapter 8

A summary of the work covered in this thesis is presented in this chapter. Conclusions on the work accomplished and some suggestions for further work are also included.

The references cited in this thesis are numbered in the order that they appear in the text and the list of abbreviations and symbols is in an alphabetical order. The Appendix contains details of simulation of the MOV capacitor protection scheme.

CHAPTER 2

AN OVERVIEW OF PROTECTIVE TECHNIQUES FOR SERIES COMPENSATION LINES

2.1 Introduction

The increase in the complexity, interconnection and size of power systems has increased the need for fast protective schemes particularly on important lines [4]. High speed fault clearance is recognised as an effective method of increasing power transfer and improving the transient stability of a power system [4,5]. In recent years, a considerable amount of interest has therefore been focused on ultrafast fault clearance and the various means of achieving it. However, speed must not be achieved through a loss of accuracy. The two important words in protection are *dependability*, the degree of certainty that a relay system will operate correctly, and *security*, the degree of certainty that a relay system will not operate incorrectly. For many years, reductions in protection equipment operating times have been achieved

by making improvements in relay design [6,7] and by the introduction by new technologies, such as digital techniques [8]. Schemes have, however, continued to exploit basic physical principles introduced many years ago, namely current comparisons and impedance measurements.

2.2 Protection Problems Associated with Series Compensated Lines

As mentioned in the previous Chapter, the advent of series capacitor compensation has been somewhat of an economic revelation, both in terms of improving the steady state transmission characteristics of a power network and reducing its transmission losses. The cost of any power capacitor is roughly proportional to the square of the voltage that it must withstand and series capacitors become prohibitively expensive if they are to be subjected to the large voltage levels that exist during system disturbances. To protect the capacitor banks in the presence of severe overvoltages which may develop across the capacitors, predominantly under fault conditions, various types of independent schemes find common applications worldover. These are referred to as the conventional gap schemes and a non-linear Metal Oxide Varistor (MOV) scheme, the fundamental purpose of each being to completely remove or partially remove the capacitor from the system, by by-passing or diverting the line current flowing through the latter. These schemes are described in detail in a later section.

The action of by-passing a series capacitor results in rapid changes in the effective system impedances. Moreover, it is impossible to predict both the exact number and

the precise instant in time at which the various capacitor protection circuits will operate. The reason for this is that under fault conditions, there are a vast number of variables which affect the magnitude of overvoltages. These include fault loop resistance, pre-fault loading, source phase sequence ratios as well as capacities,point on wave at which fault occurs, type of fault, etc [9]. Because of this degree of uncertainty, series compensated lines pose difficult problems for the conventional line protection relays, particularly those that are based on non-unit principles [10,11].

2.2.1 Problems with Conventional Protection

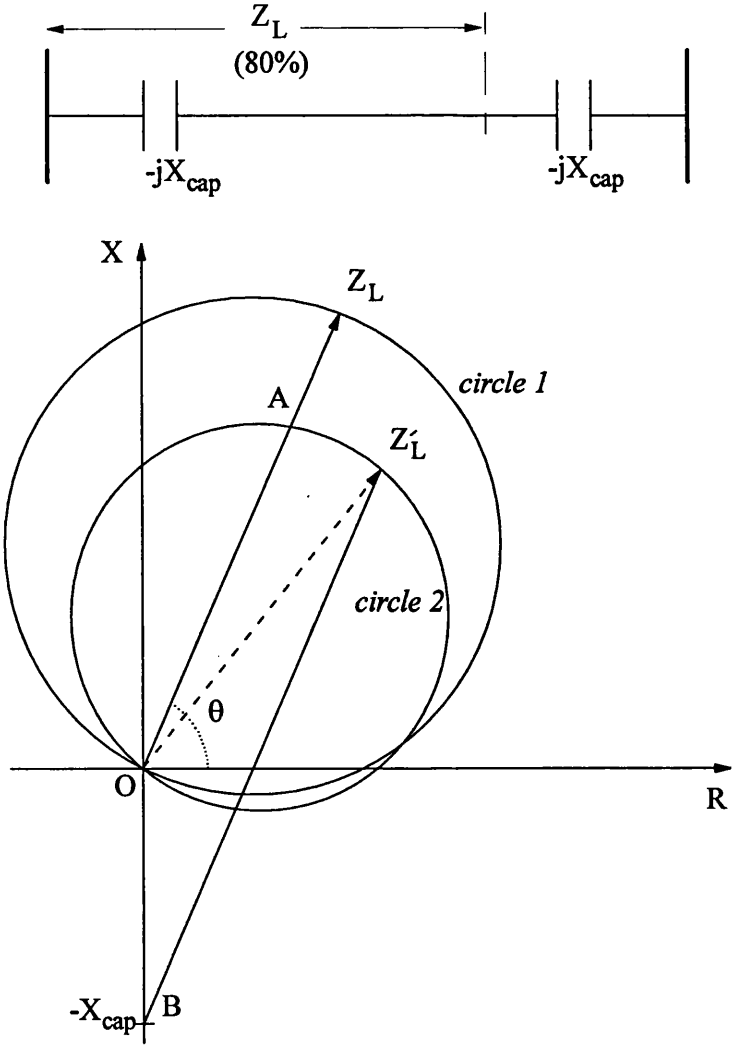
Most conventional protection schemes for EHV transmission systems rely on extracting voltage and current signals around the power system frequency to detect faults [8,12]. *Non-unit* protection schemes use only locally derived information to detect faults and distance relays are the most common type. These use the instantaneous current and voltage signals to calculate an impedance values [13]; this corresponds to a distance measurement because the power conductors have a fixed impedance per unit length. In simple terms, if the impedance seen by the relay is less than the line impedance, then an internal fault is indicated, and if it is greater, then the fault is external to the relay.

The application of distance relay to a system with series compensated lines is, however, considered to be one of the most difficult tasks for relay manufacturers. For example, the distance relay reach measurement depends upon the status of the capacitor and the transient response of the capacitor protection circuit. As mentioned

previously, the operation of the latter, in general, does not conform to any pre-defined pattern. If a capacitor(s) is protected by a conventional gap scheme, the operation of the latter results in all the compensation being removed from the system. On the other hand, if a capacitor is protected by a non-linear MOV element, there is always some compensation (which is variable) present in the system and the level present is dependent upon the location of the fault. Thus, due to the varying amount of capacitance in the circuit and additional transients being introduced, distance relays will have a tendency to maloperate.

A typical example is shown in Figure 2.1, which shows one of most common type of distance relay characteristics employed called the *Mho impedance characteristic*. The diameter of circle 1 corresponds to the impedance setting (or reach, Z_L) without series compensation and it is rotated according to the line impedance angle, θ. If the measured impedance falls within the boundary of the circle, a trip decision is issued. The situation with series compensation is indicated by circle 2. It should be noted that, the reach of a distance relay cannot be set to the length of the line because of the inaccuracies of the impedance measurement. Therefore, the relay typically has three time graded zones: zone one covers 80% of the protected line; zone two covers 150% the protected line and zone three covers 225% of the protected line, and 10% behind the line. Typically, zone one operates instantaneously, zone two operates after about a 0.3 sec delay and zone three is delayed by approximately 0.5 sec [14]. As shown in Figure 2.1, if the relay is set with Z_L' characteristic (ie assuming capacitor is always in the circuit) then if subsequently there is a capacitor flashover under a fault condition, the line impedance changes to Z_L. This effectively means that the

protection relay would protect only OA part of the line and which is less than 80% of the line length; ie there would be underreaching. On the other hand, if the relay is set to Z_L characteristic (ie. set with capacitor out of the circuit and subsequently there is no flashover of the capacitor under a fault), then the line impedance stays on Z_L'. This effectively means that the relay would detect faults beyond the 80% mark, ie. there would be an overreach.



OZ_L - Solid fault impedance locus without series compensation

OZ_L' - Solid fault impedance locus with series compensation

Figure 2.1 Mho characteristic : capacitor at each end of the line

Digital distance protection schemes allow much more complicated trip criteria to be established. The trip characteristics are normally made up from a number of straight lines forming a quadrilateral, rather than based on a circle. However, they do not overcome the problems with boundary accuracy and setting the reach points, particularly with complex power networks such as series compensated systems [15]. In general not all series compensated lines are identical. The major variables for protection are the degree of compensation, the capacitor position (and whether it is split into two parts), the type of overvoltage protection and its operating level, and the location of the relay measuring transformers. Because of all these uncertainties and differences amongst series compensated lines, such lines pose difficult protection problems for line relays. Any mode of independent tripping without the use of communication channels linking the protection at two ends, is often unsatisfactory.

Moreover, transients associated with series capacitor gap firing can also affect power line carrier operation in schemes operating in a dependent mode, ie. *Unit* protective schemes. The voltage generated in the capacitor discharge circuit can produce an erroneous power line carrier signal, resulting in misoperation of carrier relaying [16]. EHV lines with series compensation are also difficult to protect with conventional directional comparison relaying schemes. If series capacitors are located at the ends of the transmission line, and fault currents are not large enough to flash the capacitor protective gaps, faults just beyond the capacitor bank on either the protected line or on external lines appear to be in the reverse direction on a steady state basis [17]. Phase comparison has the advantages that only currents are used and therefore it is not affected by voltage reversals that can be introduced by the series capacitor [18].

However, special consideration must be given to schemes which use weighted sequence currents generated by sequence networks. Phase impedance unbalance due to unsymmetrical gap flashover can result in angular differences between the sequence quantities at the two ends of the line and can cause failure to trip or unnecessary tripping if not properly allowed for. Schemes which employ a separate relay for each phase do not have this problem, but require special channel considerations and costs can be very high with this approach.

One very common method of protecting series compensated lines involves the use of distance relays operating in a directional comparison mode in conjunction with either carrier or microwave signalling channels. For systems with less than 50% series compensation and a capacitor located at the midpoint of the line, such a protection scheme can offer reliable operation [10]. However, these types of communication channels are expensive and the protection schemes can lose integrity if a channel fails. When the capacitors are located at the line ends, directional comparison schemes using distance relays are not very satisfactory, because of forementioned voltage reversal at the relay location. In the case of double circuit applications, both voltage and current reversals are quite common. A distance relay employing an expanded characteristic of the *Fully Cross Polarised Mho* type, goes some way to solving the inversion problem, but the degree of expansion is very dependent upon the type of fault and the impedance ratio of the local source to the series capacitive reactance [10].

Another method is a directional voltage blocking scheme. This has been successfully

implemented in conjunction with distance relays to block any mal-operation of the latter in the presence of voltage inversion alone. However, when both current and voltage inversion occurs, although a correct decision is available from the distance relay, nevertheless an unnecessary block is initiated by the directional voltage blocking relay. Therefore, the range of applications for which such a scheme is suitable is somewhat limited.

Another approach has been adopted by Matthews and Wilkinson [19], namely a directional comparison protection system suitable for compensated and plain feeder systems, which has two main measuring relays to determine the direction for all fault types. The first is a positive sequence distance relay with a Mho characteristic, which provides protection for three phase faults. The second is a negative sequence directional relay which provides protection for all unbalanced faults. Each relay has a trip and block element. It is designed such that for an internal fault, the trip relay operates before the block relay and by-passes any action taken by the latter. The opposite procedure occurs for the external faults. There is a polarising quantity correction factor which is introduced to neutralize the effect of polarising voltage inversion at the relaying point. However, this factor is determined by the specific ratio of source reactance to the series capacitive reactance. Thus, this type of protection scheme may not perform satisfactorily in a practical series compensated system, since an effective value of the source capacity and hence impedance behind the relaying points, is not always known and depends entirely upon the number of infeeding lines and the number of generators connected to the local bus.

A commonly encountered problem with series compensated line protection arises due to the presence of subsynchronous currents that are introduced into the system when the capacitor protective gaps do not flashover [16,20]. Such waveform distortions can cause improper relay operation if not catered for in the relay design. It is therefore of utmost importance that any line protection equipment should detect the presence of a fault on the system with minium delay. If this is achieved, rapid breaker opening could then prevent any damage to power system plant by disconnecting the faulted line section.

2.3 New Types of Protection schemes

Recently some researchers [21,22] have resorted to new digital techniques in impedance measurement which employ adaptive relaying; this can be simply defined as a type of protection which permits and seeks to make adjustments to various protection functions in order to make them more attuned to prevailing power system conditions. This is often achieved by dynamically changing the relay setting to accommodate the most conceivable network conditions. Considerations of various problems encountered in impedance protection systems as applied to series compensation lines make such adaptive approach sometimes deficient since not all possible system contingencies can be anticipated during the design of the protection system.

2.3.1 Travelling-Wave Based Protection

During the last few years, considerable interest has been shown in the possible use of travelling wave relays to fulfil requirements of modern bulk EHV transmission networks with long lines [23,24]. These techniques are based on the transmission line travelling wave theory and these can be usefully applied for relaying purposes as shown in Figure 2.2. Obviously, a directional comparison relaying scheme would be possible if the direction of motion of the travelling waves could be recognized at terminals A and B.

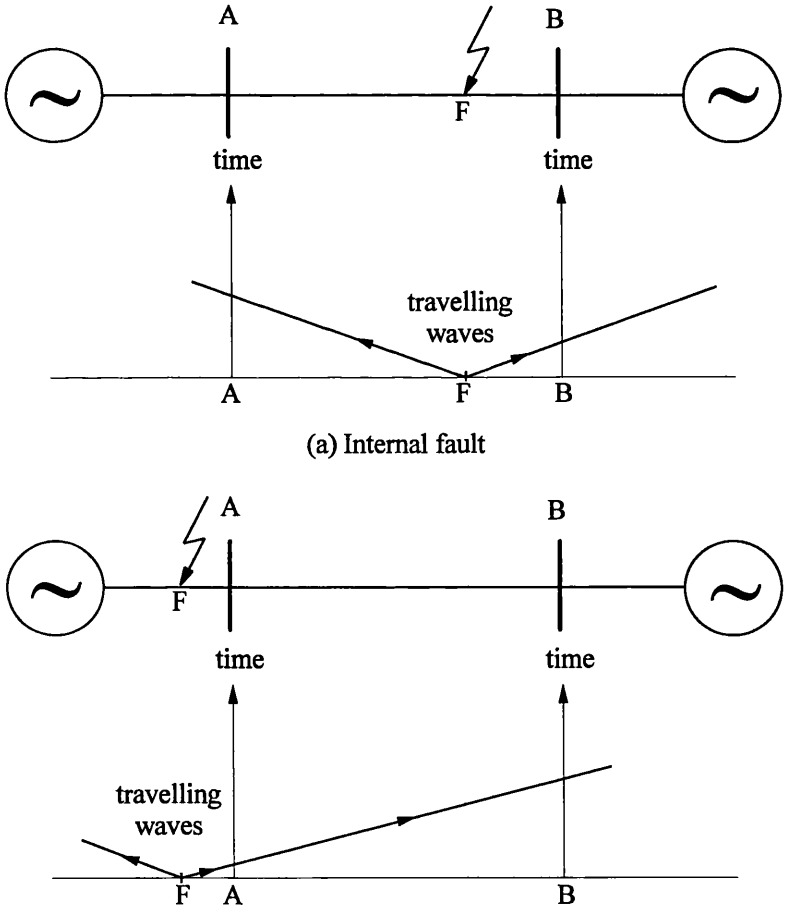


Figure 2.2 Propagation of the travelling waves

Using the travelling wave concepts and observing the sign of the voltage wave with respect to the current wave or their superimposed components immediately after a fault, a directional discrimination to the fault can be determined. Also comparing the magnitudes of the forward incident wave and reverse wave in the time domain, the distance to a fault can be estimated. The travelling wave relays are attractive because they offer, at least in principle, the possibility of a true UHS response.

Chamia and Liberman have, in conjunction with the Swedish company ABB [24], produced a directional wave detection device called RALDA which has been installed for plain feeders in many countries worldwide. A directional decision is based upon the relative polarities in the measured voltage and current changes at the two ends of a protected line section, the protection at the two ends being linked via a communication channel. This dependent mode of operation, configured as a blocking mode unit protection scheme is complemented with underreaching elements at each end, providing high speed independent operation, a desirable aid to rapid clearance of high level close up faults. However, such a scheme has its drawbacks in that its underlying principles are based upon an unqualified assumption. The voltage and current components are examined on a per phase basis ie segregated phase, which is perfectly acceptable for single phase networks. However, it is well known that in polyphase systems, the healthy phases, because of mutual coupling, are greatly affected by the current and voltage changes in the faulted phase. This means that under certain external fault conditions, the components induced in the healthy phases at the relaying point can be indicative of either a forward or internal fault to such a scheme. When applied to series compensated systems, although such a scheme will

have the distinct advantage (over conventional protection) in that, in a majority of practical applications, it would operate before any capacitor protective gap flashover, however, the aforementioned mutual coupling problems can be aggravated since large fault current levels are generated for such lines than those associated with plain feeders. In addition, a simple comparison of the relative polarities of the voltage and current changes is not a totally reliable method of determining the direction to fault when a blocking mode protection scheme is employed. The RALDA scheme, although not an impedance measuring device which makes it attractive for series compensated systems, does not, however, offer total reliability of operations for all series compensated systems.

In recent years schemes utilising travelling wave techniques, suitable for series compensated lines, have been developed [25]; those are based on the work initially carried out by Johns [26]. The basic relay operating principle relies upon deriving two composite superimposed signals using modal voltages and currents at each end of a feeder. The use of the modal quantities eliminates the mutual coupling between the phases of a transmission line. The criteria for determining the direction to fault is based on the fact that for an internal fault (fault on protected line) the superimposed modal voltage and current components are of opposite polarities at each end of the feeder. A forward fault indication is thus given by both relays and which is sent to the other end via a communication link. Conversely, for an out of zone fault, although the relay at one end gives a forward fault indication, however, the modal voltage and current components at the other end are of like polarity resulting in a reverse fault indication by that relay which in turn sends a block signal.

This scheme also relies heavily, as any other directional comparison scheme, on the communication link between the two ends of the line.

Each of the foregoing techniques operates on the unit principle but the speed of overall fault clearance depends on the speed of the signalling channel. Some recent work by Thomas and Christopoulos [27,28] examines the possibility of a non-unit approach. Such schemes basically depend on detecting the magnitudes of the first voltage and current waves to arrive at the end of a line after the incidence of a fault. The magnitudes of subsequent voltage increments are then processed to achieve the necessary discrimination. However, schemes based on the travelling wave phenomena have been considered failures for near zero degree of fault inception angle. Some work has also shown that even though the initial voltage and current increments are large enough to be detected, some of the subsequent increments may be small because of the reflection coefficients. This would appear to be a serious limitation of such a scheme.

2.3.2 Non-power Frequency Component Protection

The use of non-power frequency components for protection measurements is an area that has received relatively little attention. However, more recently, some work has been done on using non-power frequency components of currents in the detection of low level faults in distribution systems [29, 30, 31]. These exploit the wideband noise signals that are emitted by arcing faults. Mehdi [32], investigated the feasibility of using fault generated HF current signals (typically 100 kHz) for the ultra high speed

protection applications. For discrimination purposes, wave-traps on the primary side of the transmission line have been used. The disadvantage of this techniques is that it requires a special wideband current transducer. Later, Johns [33] proposed an alternative technique that utilised HF components impressed on the system by faults and derived from a tuned circuit connected to a conventional CVT. The tuned circuits are arranged to act as HF switched stack tuners and the technique is dependent on conventional directional detectors to perform the necessary HF stack-tuner switching. However, the latter is subject to the usual limitations of conventional power frequency signal measuring equipments. As such, there is a limit to the sensitivity of such a scheme, in particular to high impedance faults. More recently, the principle of this technique has been developed to produce a discriminative non-unit protection scheme for plain EHV transmission lines [34,35]. The work presented in this thesis expands this technique further to protect the series compensated lines. The primary purpose of this work is thus to outline the progress made in the further design, development and application of the aforementioned non-power frequency voltage signals to series compensated lines. Particular emphasis has been paid to evolving a design that overcomes the foregoing practical problems associated with the protection of series compensated transmission lines.

CHAPTER 3

BASIC PRINCIPLE OF THE NEW PROTECTIVE SCHEME

3.1 Introduction

This chapter describes the basic principles of the new protective scheme for series compensation systems. The relaying scheme is based on utilising the fault-induced HF signals at any one end of the line. This chapter also describes how the high frequency voltage signals are captured and the high voltage equipment that is required to do so.

3.2 Signal Measurement Technique

Most conventional protection relays for fault detection only involve processing information based on the derivation of the fundamental (power) frequency components of post-fault current and voltage [8]. Sudden changes in the power system voltage that occur in the immediate post-fault period, due for example to

arcing faults and travelling waves, create wideband high frequency (HF) signals on the associated EHV power lines [36, 37]. These HF signals can be used for protection purposes [38], but they are generally outside the bandwidth of receptability of most conventional voltage transducers. Recent works [33, 39] have shown that the HF signals of interest can be detected using power line carrier (PLC) communication equipments [40] and these can be very effectively utilised for designing alternative forms of protection devices. A stack tuner is used to capture the relevant signals while a PLC signal line trap confines them to the protected zone and gives the technique its discriminative properties. This arrangement is shown in Figure 3.1 and is connected to all three phases at each end of the line to be protected. Typically, HF coupling equipments comprise two couplings, one to each of the two of the primary conductors, called phase-to-phase coupling [41]. Therefore, an additional line trap and tuner would have to be fitted to the third conductor for it to be suitable for this fault generated noise protection scheme.

The stack tuner is connected to the coupling capacitor, C_C , of a standard capacitor voltage transformer (CVT). The stack tuner unit is a parallel RLC network and is designed to capture a narrow band of high frequencies around a specified centre frequency. It offers a very high impedance at the power frequency (50 Hz) and has an impedance very close to the line characteristic impedance at the tuned centre frequency. The stack tuner thus permit HF signals to pass with minimum loss and protect the measurement system from dangerous overvoltages by isolating it from the high voltage potential of the transmission line. For most practical purposes, it can be

assumed that the stack tuner acts as an open circuit at the power frequency. The coupling capacitor is used to provide a voltage proportional to line voltage for the operation of protective relays and other instruments.

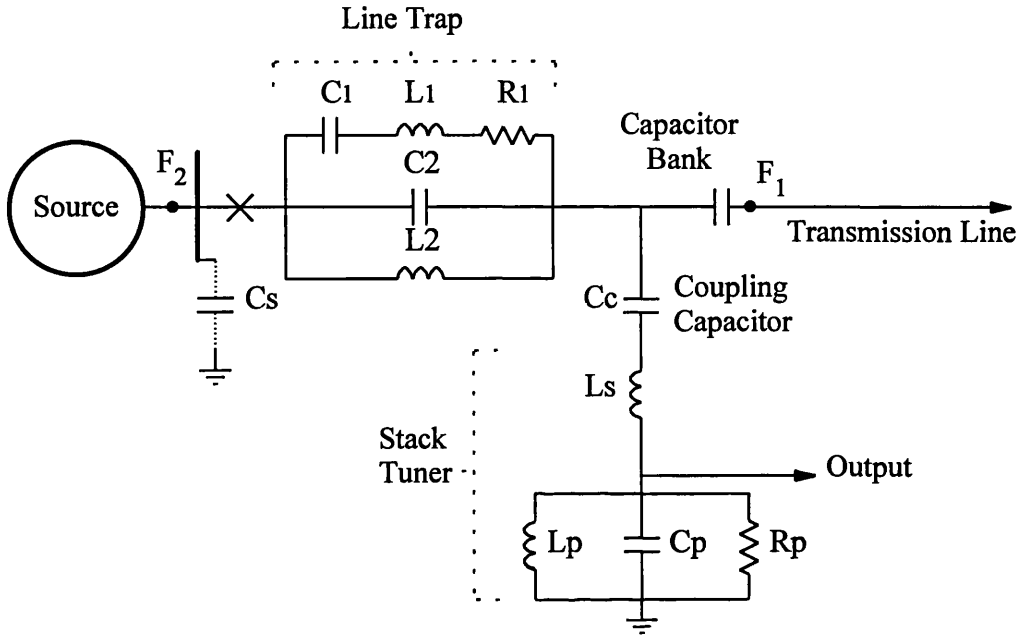


Figure 3.1 Line trap and stack tuner arrangement

The line trap is the standard type used in PLC application by the National Grid Company (NGC) in Britain and it consists of a series RLC network in parallel with a parallel LC network and so behaves as a bandstop filter. That is, the line trap is tuned to block a narrow band of high frequencies by offering a high impedance around a specified centre frequency while offering a very low impedance at all other frequencies. The line-trap unit is arranged to have an impedance provided by R_1 of approximately ten times the line characteristic impedance at the centre frequency. This value of R_1 is necessary to attain better discrimination between internal and external faults. All line traps are tuned to the same centre frequency.

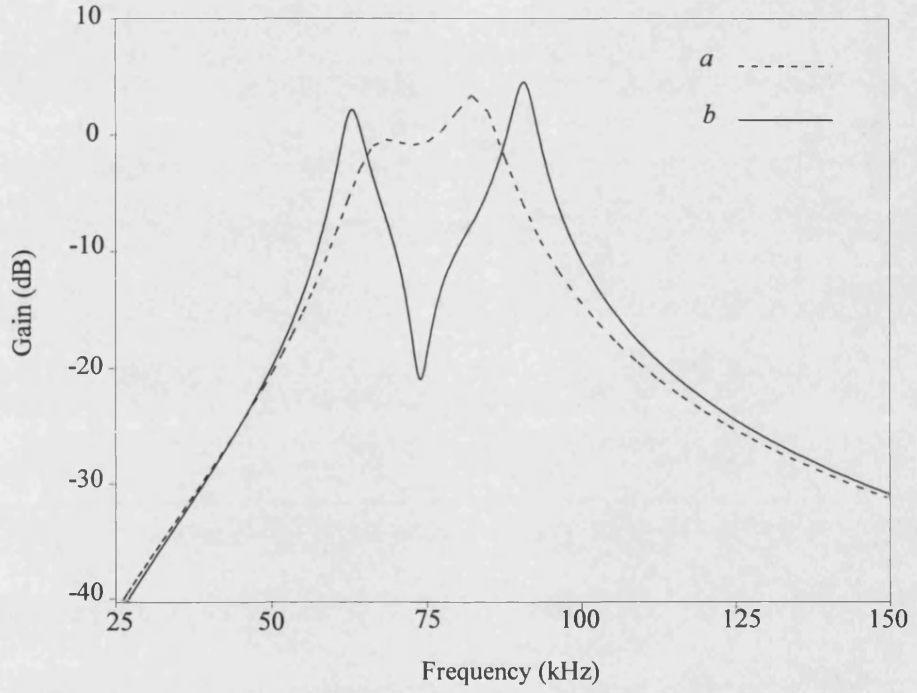
A number of studies [33, 42] have been done to determine the most suitable frequency band for the protection scheme. It should be mentioned that practical considerations play a significant role in the choice of the centre frequency as this affects the sampling frequency required and therefore the time in which all the relay's calculations have to be completed. Considering currently available Microprocessor hardware, it was ascertained that a 5 μs interval between samples would be sufficient time to carry out the required protection algorithmic calculations and so a sampling rate of 200 kHz was chosen. Therefore, the highest frequency that can be detected from the stack tuner is 100 kHz according to the Nyquist sampling theorem. The line trap and stack tuner were tuned to the National Grid PLC Communication Band 1 (70-81kHz) with a centre frequency of 75 kHz and the parameter values for this band are shown in Table 3.1.

Table 3.1 Line trap and stack tuner parameters

Line Trap		Stack Tuner	
Parameter	Value	Parameter	Value
C_1	1.12 nF	C_C	2.0 nF
L_1	3.97 mH	L_S	2.1 mH
R_1	2700 Ω	R_P	270 Ω
C_2	24.8 nF	C_P	35.3 nF
L_2	185 μH	L_p	133 μH

In Figure 3.1, C_S is the stray shunt capacitance at each busbar and a typical value of 0.1μF was used in the simulation. It provides a low impedance path to ground over all frequencies within the defined frequency band centred on 75 kHz. Figure 3.2

shows the overall frequency response of the line trap and stack tuner arrangement, both for forward voltage input, ie. an input voltage in front of the line trap at point F_1 in Figure 3.1, and for a reverse voltage input, ie. an input voltage behind the line trap at point F_2 in Figure 3.1.



a For forward-voltage input (internal, at F_1)
b For reverse-voltage input (external, at F_2)

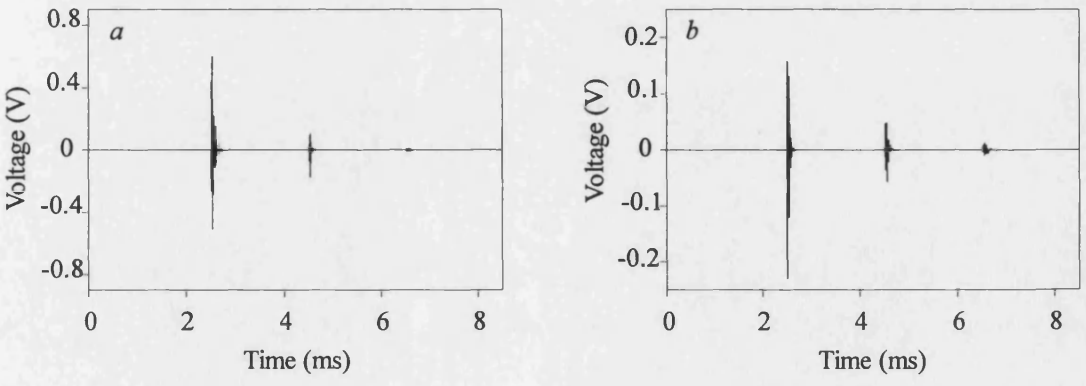
Figure 3.2 Overall frequency response of the line trap and stack tuner

It is apparent that, as expected, in the first case, there is very little attenuation (the gain stays near 0 dB) over the tuned frequency band and increasing attenuation on either side, but in the second case, there is very severe attenuation (the gain falls to about -20 dB) over the tuned frequency band. The latter can be attributed to the short circuit effect of the stray capacitance C_S and also to the very high impedance offered

by the line trap around the tuned band. It is these characteristic features of the signal measurement circuit which form the basis of discrimination between internal and external faults.

3.3 Relay Operating Principle

The basic relay operating principle hinges upon detecting the fault generated HF voltage signals by using the foregoing signal measurement circuit and can be best understood by examining some typical single phase to earth fault output waveforms. For these purposes, a double ended series compensated system with 300 km line length, 20 GVA short circuit level capacity at the sending end and 0.5 GVA at the receiving end respectively are used. The time domain outputs from the stack tuner closest to the fault are shown in Figure 3.3; these are for both internal and external faults (near voltage zero) on the line and busbar sides of the measuring equipment, respectively (at point F_1 and F_2 in Figure 3.1).

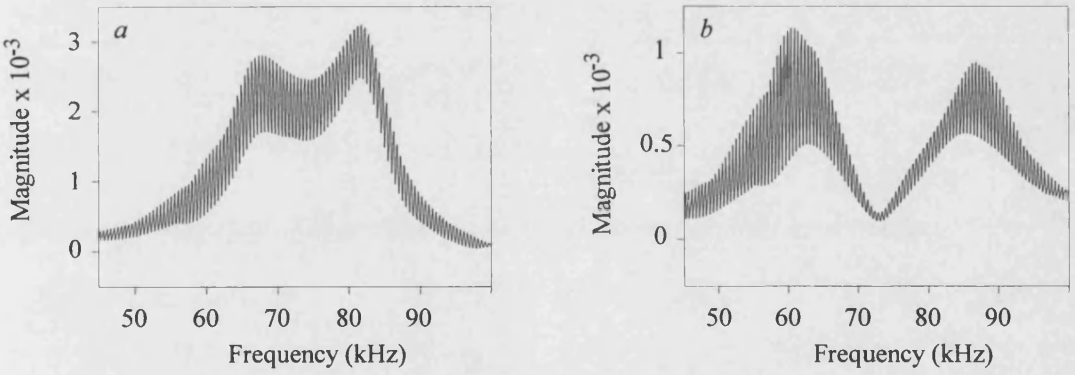


a Internal fault stack tuner output

b External fault stack tuner output

Figure 3.3 Internal and external fault time domain stack tuner outputs

These typify characteristic bursts of the HF signals and the initial burst is due to the electric arc at fault inception. The successive bursts are due to a combination of HF components generated by the nonlinear behaviour of the primary fault arc and travelling wave components; these arise due to reflections from the impedance discontinuities in the circuit such as at the fault point and line ends. In the time domain there are no obvious differences that can be observed between the two waveforms, except slight variations in the signal magnitudes. However, in the frequency domain, the severe attenuation caused by the line trap in the external fault case is clearly visible (Figure 3.4). It is this significant difference that enables discrimination between internal and external faults to be achieved.



a Internal fault frequency spectrum

b External fault frequency spectrum

Figure 3.4 Internal and external fault frequency spectra

The basic relay principle thus depends on the formation of two discriminant signals, the first called the *operate* signal based on signal energy around the centre frequency, ie. 75 kHz, and the second called the *restraint* signal based on signal energy slightly

off-centre frequency. The operate quantity is divided by the restraint quantity to form a *discrimination ratio* which determines whether a fault is in-zone or out-zone. In other words, for an internal fault, this ratio will be approximately equal to or greater than one as the operate and restraint quantities are comparable and for an external fault, it will approach zero. Finally, this ratio initiates a decision process which comprises of a counter. The latter issues a trip decision when its value exceeds a predetermined threshold level. These will be described in more detail in chapter 5, section 5.3.4.

3.4 Summary

This chapter describes the basis of a new protection technique for series compensation lines which utilises the HF components of fault-generated noise caused by arcing faults. The design features and the behaviour of the signal-measurement circuit is explained and the these form the basis of discrimination between internal and external faults.

CHAPTER 4

SIMULATION OF THE POWER SYSTEMS

4.1 Introduction

This chapter describes the simulations used to generate accurate and realistic fault data to develop the protection algorithm. The simulation of the power system has been done using the universally accepted Electro-Magnetic Transients Program (EMTP) [43]. It contains mathematical models for almost every major power system component, including nonlinear elements such as circuit breakers and surge arresters and the capabilities of this program for conducting engineering studies are enormous. The data was calculated at 1 μs intervals (ie. simulated at 1 MHz) to give improved accuracy. Every 5th data value was recorded so that the output data was accurately produced at the desired sampling rate of 200 kHz.

4.2 Primary Arc Model

Faults in power transmission systems often take place through long arcs in air. Therefore, a realistic simulation of fault arcs is extremely important in the successful design and development of novel protection schemes [44]. An electric arc model was included in the simulations to produce accurate fault data and the Transient Analysis of Control Systems (TACS) subsection of the EMTP was used for this purpose. At each time step, the electrical network is solved and the relevant information is transferred to TACS. This subsection is then executed and the data from this is then used to solve the electrical network for the next time step. This process is then repeated for the duration of the simulation.

Following a fault on a transmission line, an electric arc develops which is very often across the line insulator string. The primary arc exists from the time of fault inception to when the circuit breakers open. This becomes a secondary arc once the circuit breakers have opened, isolating the faulted conductor (in single pole tripping) and which is maintained by the mutual coupling between the faulted phase and the sound phases. The studies here are only concerned with what happens during the primary arcing time.

It has been a long tradition that the primary arc be simply represented by an ideal short circuit, or by a low value linear resistance [45]. However, if the transients produced by arcing faults are to be predicted realistically, then the fault arc has to be represented as accurately as possible. In this respect, Reference [36] represents the

fault arc by a piecewise arc characteristic. The arc model used here, is based on the energy balance in the arc column that was first developed by Hochrainer [46] and the non-linear behaviour of the primary arc is fundamental to this work. Control system and switching arc theories have been applied to this to describe the dynamic arc characteristics [47] and it can be exactly simulated by the following arc equation:

$$\frac{dg}{dt} = \frac{1}{\tau}(G-g) \tag{4.1}$$

where g is the time varying arc conductance, G is the stationary arc conductance and τ is a time constant. The stationary arc conductance G can be physically interpreted as the arc conductance value when the arc current is maintained for a sufficiently long time under constant external conditions. Thus, the static characteristic of the arc, G, can be evaluated by:

$$G = \frac{|i|}{(V_o + R|i|)l} \tag{4.2}$$

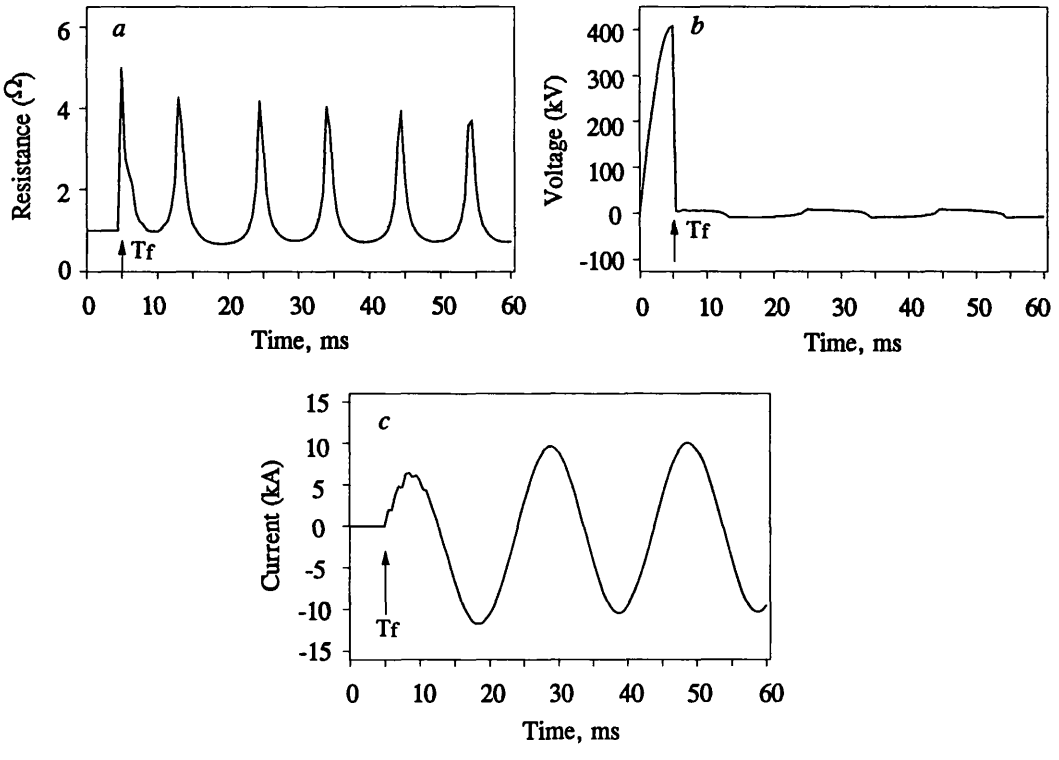
where i is the arc current, V_o is the constant voltage parameter per unit arc length, R is the resistive component per arc length and l is the time-dependant arc length. The time constant τ and the length of the arc l in equations 4.1 and 4.2 are considered to be constant during the primary arc and the parameter values have been determined from the experimental data discussed in reference [47].

The arc is represented by a time-varying arc conductance which is computed using the measured arc voltage and current at discrete time points. The dynamics of the arc is represented by a block diagram in the program part TACS. The arc equation

(Equation 4.1) is solved at each time step using the following equation (Equation 4.3), by making the assumption that the time constant and stationary arc conductance remain constant during each time step.

$$g(t) = G(t-\Delta t)-[G(t-\Delta t)-g(t-\Delta t)]\exp(-\frac{\Delta t}{\tau}) \qquad (4.3)$$

The reciprocal of this then gives the time varying arc resistance which is used to represent the arc in the simulation. The electric network and the control system are solved separately in the EMTP and TACS program respectively at each time step using the data from the previous time step. The simulation always started from the steady state condition and some relevant waveforms for a typical fault using this model are shown in Figure 4.1.



a Arc fault path resistance

b Arc fault path voltage

c Arc fault path current

Fault inception, T_f = 5 ms

Figure 4.1 Non linear arc behaviour

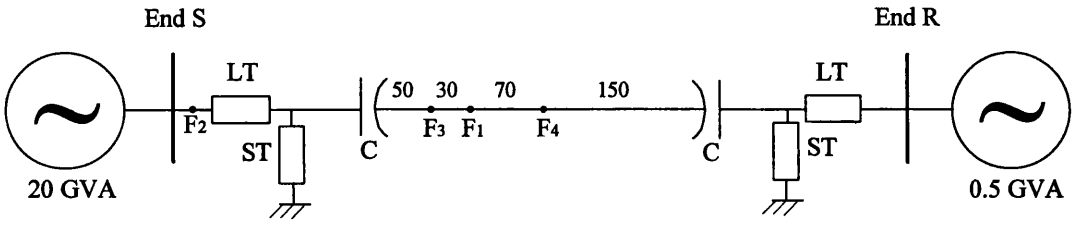
The nonlinear time varying behaviour of the arc is clearly evident from Figure 4.1a and this is in marked contrast to the conventional approach of assuming a small linear resistance in the fault-arc path. More importantly, the latter manifests itself into distorting the fault arc path voltage waveform, as is evident from Figure 4.1b. It is this distortion which is particularly responsible for generating the HF noise in the signals at a rate of two per cycle of power frequency period and this is due to the arc restriking as it passes through a current zero (Figure 4.1c); the time of the restrike will depend on the amount of dc offset in the current waveform and this is strongly influenced by the fault inception angle. In this case, the restrike occurs every 10 milliseconds as there is no dc offset associated with this voltage maximum fault. As expected, the effect of the non-linear arc has little bearing on the fault arc path current; this is so because the level of the distortion, relative to the power frequency components in the current, is much smaller and therefore gets completely swamped over by the latter. It should be mentioned that the additional HF signals are also generated with every restrike giving the protection technique further opportunities to correctly identify the fault and the scheme therefore does not rely on the presence of travelling wave components which are heavily dependent upon fault conditions such as fault inception time, fault location etc.

4.3 Power System Configurations Studied

The simulation results presented in Chapters 6 and 7 are based on the different network configurations shown in Figure 4.2 with the series compensated main line S-R; here symbol 'End S' represents the busbar name closest to the sending end relay

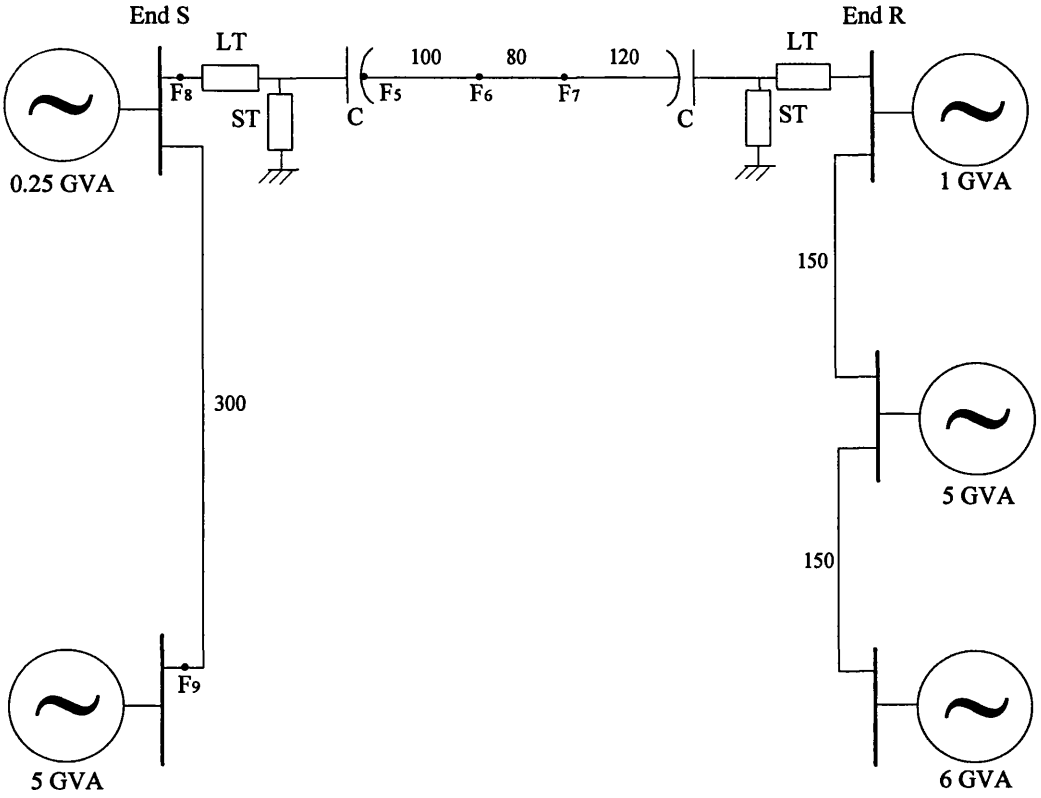
and 'End R' represents the busbar name closest to the receiving end relay. All systems comprise 500 kV, single circuit transmission lines and an X:R ratio of 30 and Z_{S0} : Z_{S1} ratio of 1 were used for each source terminating a busbar.

There are a large number of possible capacitor locations and degrees of series compensation encountered in practice. However, the two most common systems are [9]: a single capacitor bank located at the middle of the line and a capacitor bank located in the vicinity of each line end. Of the two, although the former is economically less viable, however, from a line protection point of view, it is generally more easily protected and does not pose any major problems with modern protection relays. The latter system, however, although economically very attractive, poses some of the most difficult protection problems for conventional protection relays. Therefore, the results presented herein are mainly for the system where a capacitor is located near each line end and a typical level of compensation of 70% is used throughout. However, some results are also presented for the system where a capacitor is located at the middle of the line with a typical level of compensation of 50%. The arrangements for these systems are as shown in Figures 4.2a to 4.2d.



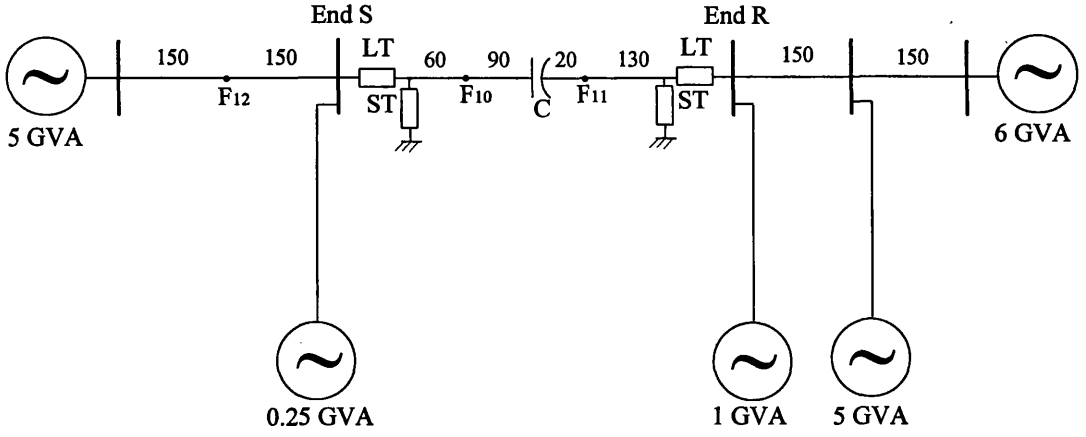
All distances in km LT - Line Trap ST - Stack Tuner

Figure 4.2a Single section feeder, with 70% series compensation



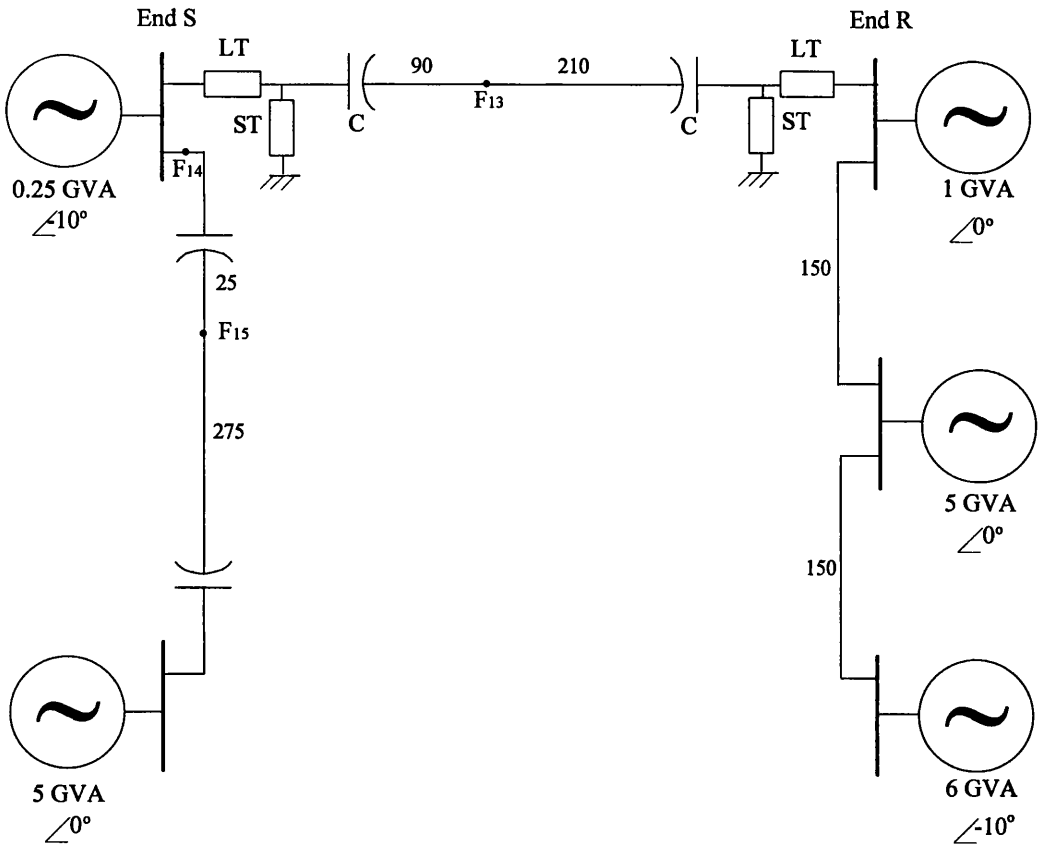
All distances in km LT - Line Trap ST - Stack Tuner

Figure 4.2b Multi-section feeder, with 70% series compensated main line S-R



All distances in km LT - Line Trap ST - Stack Tuner

Figure 4.2c Multi-section feeder, with 50% series compensated main line S-R



All distances in km LT - Line Trap ST - Stack Tuner

Figure 4.2d Multi section 70% series compensated feeder system

a, b and *d* : Compensation at line end; *c* : Compensation at the midpoint

Figure 4.2 Power system configurations studied

The system of Figure 4.2a is a single section feeder system in which the terminating sources comprise of a general source model based upon arbitrarily defined short circuit levels. The extreme source capacities of 20 GVA and 0.5 GVA indicated are unlikely to be encountered in practice, especially with a continuous line section of 300 km between the two ends. However, it is a good, simple example to clearly demonstrate the performance of the proposed relay scheme.

Considering the multi-section typical EHV feeder system arrangements shown in Figures 4.2b and 4.2c, the combination of infeeding and local generation behind busbars S and R, have different source capacities at each end. There is no phase shift between the voltages at each end. The system simulations have also been extended further to include more complex and therefore more realistic power system networks (Figure 4.2d), in order to demonstrate the performance of the relay technique developed herein under practical situations. This circuit has a series compensated infeeding line in addition to the main compensated line S-R. Also the source voltages at End S lag the End R source voltages by $\angle 10^0$, and the far receiving end voltages lag the End R voltages by $\angle 5^0$. This is to represent some initial power flow around the network.

4.4 Transmission Lines Configuration and Parameters

The EHV transmission line modelled used in this simulation is based on a typical single circuit 500 kV horizontally constructed line commonly employed in long distance transmission application in many overseas countries [48]. Details of the overhead transmission line configuration are given in Figure 4.3 and the distances of the conductors above the ground are average values taking into account the catenary (ie. conductor sag) of the span between two consecutive towers.

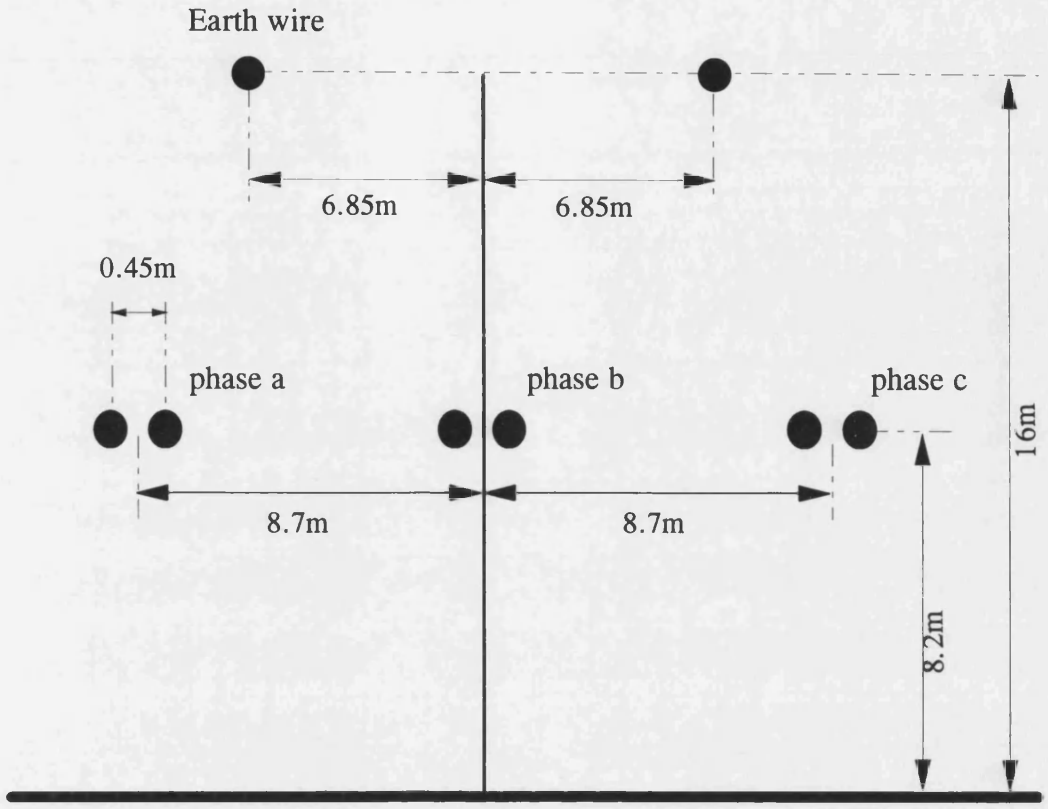


Figure 4.3 500 kV single circuit transmission line construction

4.4.1 Phase Conductors and Earth Wires

Phase conductor type is aluminum conductor, steel reinforced (ACSR), which consists of layers of aluminum strands surrounding a central core of steel strands. Earth wires located above the phase conductors protect the phase conductors against lightning. They are usually high- or extra-high-strength steel, Alumoweld (Aluminum-Clad Steel), or ACSR with much smaller cross section than the phase conductors. Due to the horizontal construction, the material of the earth wire is Alumoweld, which is known to be approximately 25 times more resistive than ACSR phase conductor.

In the line system simulation model, the conductor parameters are taken from the EHV Transmission Line Reference Book [49], as follows:

(1) Phase conductors are 2×84/19/0.35cm ACSR with 45.72 cm bundle spacing (Code: Chukar).

(2) Earth wires are 7/0.35 cm Alumoweld (Code: 7 No. 9)

(3) Earth resistivity is 100 Ωm.

(4) Conductor resistance is 0.0321 Ω/km.

(5) Earth wire resistance is 1.8769 Ω/km.

(6) Conductor overall diameter = 4.0691 cm.

(7) Earth wire overall diameter = 8.712 mm

In long transmission lines, if the spacing between phases are unequal, unbalanced flux linkages occur, and the phase inductances are unequal. Therefore, to restore balance, the conductor positions along the line are exchanged (transposed) at two locations such that each phase occupies each position for one-third of the line length. In practice, it is not common to build overhead lines with transposition towers for economic reasons. Therefore, the transmission lines are not transposed and this is reflected in the modelling.

The parameters of transmission lines are dependent on the frequency at which they are evaluated. The transmission line is simulated by L. Marti's frequency dependent line model within the EMTP package [50]. Using the frequency dependent line models in the EMTP is always a two step process. The first step is to obtain frequency dependent parameters of the line based on the physical characteristics of

the line, and the second step is to incorporate this model into the EMTP simulation. A nominal power system frequency of 50 Hz was used.

Symmetrical components for the above configuration of overhead conductors are separately derived by using the EMTP "Line Constant" program. These are necessary for determining the parameter for the series capacitor and this will be described in detail in section 4.7. Some typical parameters at power frequency are shown in Table 4.1.

Table 4.1 Basic computed parameters of the line model

Sequence	Resistance Ω/km	Reactance Ω/km	Susceptance mho/km
Zero	3.02354×10^{-1}	9.87522×10^{-1}	2.75263×10^{-6}
Positive	1.72085×10^{-2}	3.03632×10^{-1}	3.88293×10^{-6}

4.5 Source Modelling

The source network can generally be represented by the Thevenin equivalent circuit of a voltage source in series with a source impedance. The source will have mutual impedance, X_m and self impedance, Z_{se} and also have positive phase sequence impedance, Z_1 , negative phase sequence impedance, Z_2 and zero sequence phase impedance, Z_0. In a practical EHV transmission line system, sources with a wye connection generally have a return path, either through the ground or a neutral conductor. Figure 4.4 shows an equivalent circuit of a three phase wye-connected source.

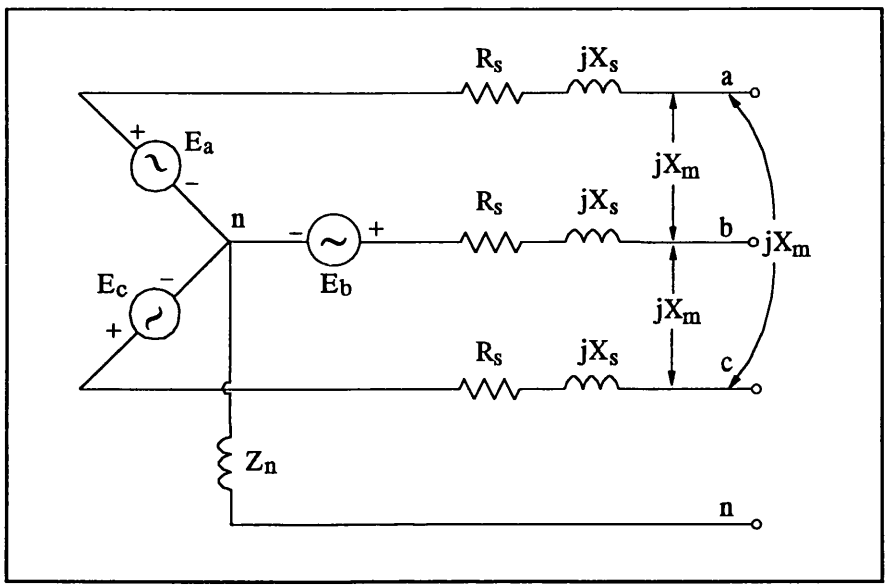


Figure 4.4 Equivalent three phase source circuit

Here (R_s+jX_s) is source impedance of each phase, jX_m is the mutual impedance and Z_n is the neutral impedance. It should be noted that the zero-sequence currents (I_0) can only exist in a circuit if there is a complete path for their flow. In this respect, a wye-connected load with solidly grounded neutral provides a return path for the zero-sequence currents flowing through the three phases and their sum, $3I_0$, flowing through the ground. If the neutral is grounded through neutral impedance, Z_n, an impedance of $3Z_n$ should be inserted between the neutral point 'n' and the ground. The reason for this is that a current of $3I_0$ produces a zero-sequence voltage drop of $3I_0Z_n$ between the neutral point 'n' and the ground.

Based on the technique outline in reference [51], the zero, positive and negative sequence impedance of the circuit can be evaluated; essentially, these are the following two Equations:

$$Z_0 = R + j(X + 2X_m) + 3Z_n \quad (4.4)$$

$$Z_1 = Z_2 = R + j(X - X_m) \quad (4.5)$$

If the mutual impedance, X_m , is very small, and the source capacity of short circuit level (SCL), line voltage (500 kV), source X:R ratio and Z_{s0}:Z_{s1} ratio are given, then the neutral impedance Z_n can be easily obtained from Equations 4.4 and 4.5.

4.5.1 Evaluation of Source Parameters

The information about the source is practically given in terms of short circuit level (SCL), X:R ratio and Z_{s0}:Z_{s1} ratio. Here each phase of the power system source was modelled as a voltage source in series with a lumped resistance and inductance to represent the short circuit capacity of the terminating busbar. The neutrals of the three phases were assumed all solidly grounded to give a Z_{s0}: Z_{s1} ratio of unity. A source X:R ratio of 30 was assumed throughout the studies and was calculated as follows:

$$Z_s = \frac{V_L^2}{SVA} \quad (4.6)$$

where Z_s is the source impedance (Ω), V_L is the operating line voltage (V) and SVA is the source short circuit level in VA.

The source resistance, R_s (Ω) and source reactance, X_s (Ω) can then be calculated from:

$$Z_s = R_s + jX_s \quad (4.7)$$

$$X_s = Z_s.\sin[\tan^{-1}(X{:}R\ ratio)] \tag{4.8}$$

$$R_s = \frac{X_s}{X{:}R\ ratio} \tag{4.9}$$

4.6 Series Capacitor Protection Schemes Employed

Series capacitors in a transmission circuit are subjected to both steady state and transient currents as the system is switched, as faults occur, and as load varies. It is usually not economically feasible to design series capacitor banks that can withstand any current level to which they may be subjected [52]. This is particularly true in situations where certain fault locations may lead to a near resonant condition. Also, since the capacitor integrates the line current, the current phase shift caused by the fault and dc offset on the fault current are factors that could lead to extremely high overvoltages across the capacitor bank. Some form of overvoltage protection is therefore necessary to limit the series capacitor overvoltages to safe levels.

4.6.1 Conventional Schemes

In practice, there are a number of capacitor protective schemes in use. For reasons of economy, the conventional gap-type scheme has been extensively used for series capacitor protection against overvoltage [53]. The most commonly used spark gaps are of two types, air blast gaps and open-ventilated gaps. Air-blast gaps may give a rapid extinction and deionisation of the spark but are rather complicated because of the air-blast valve control which involves monitoring of a number of checking points.

The open ventilated gap is much simpler but requires the operation of the bypass breaker to extinguish the spark, and additionally requires a longer time for deionisation and cooling of the electrodes than air-blast gaps.

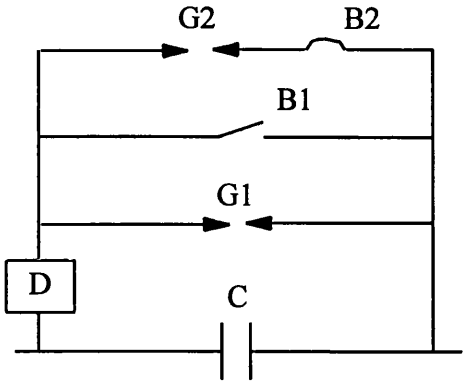
In the recent years, the open-ventilated non-self extinguishing gap has been mostly used due to its simplicity and reliability and due to the fact that it applies lower stresses on the capacitor, and thereby lower capacitor cost. For moderate demands on capacitor reinsertion speed, protective spark gaps are still the most competitive solution. Two types of capacitor protection schemes find common worldwide application which are broadly classified as follows:

(1) The dual gap scheme (DGS).

(2) The dual gap/non linear resistor scheme (DGNS).

4.6.1.1 Dual Gap Scheme (DGS)

The fundamental objective of the capacitor protection is to by-pass or shunt the capacitor with a low impedance path, thus preventing excessive voltage being developed across them. Once the capacitor voltage attains a certain threshold level, the spark gap breaks down or in other words is triggered into conduction, thereby connecting a branch usually comprising of a discharge limiting resistor and inductor, in parallel with the capacitor. Most of the line current is then diverted through this parallel path and away from the series capacitor. A schematic diagram of a conventional DGS is shown in Figure 4.5. On a three-phase installation, each phase would have an identical circuit.



C - Capacitor bank

D - Damping circuit

G1 - Spark gap , high-set (2.75pu)

G2 - Spark gap, low-set (2.2pu)

B1 - By-pass breaker

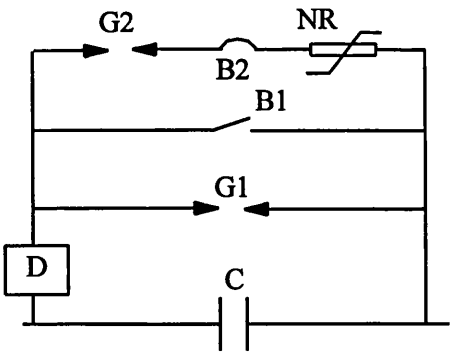
B2 - Reinsertion breaker

Figure 4.5 Conventional dual gap scheme

Ideally, the spark gap threshold level should be set high enough such that all faults external to the series compensated line section do not cause by-passing of the capacitors. As shown in Figure 4.5, the spark gap G2 (referred to as the auxiliary gap) has a lower setting than the gap G1 (referred to as the main gap), thereby allowing capacitor by-pass under external fault conditions or lower fault levels. The series breaker B2 performs the reinsertion and the damping circuit limits the magnitude of the current through the capacitor. Due to the lower gap setting of G2 compared with that of the main gap G1, this branch operates first to by-pass the capacitor. A typical setting of the gap G1 is 2.75 and that of gap G2 is 2.2 times the rated voltage (50Hz crest value). After fault clearance, the breaker B2 open circuits the dual branch, leaving the original main gap protecting the capacitor in the event of any subsequent overvoltage. In this instance, the main gap G1 is termed a *clean* gap, since it has not previously conducted any by-pass current and so has a well defined voltage withstand level. The voltage stress is totally placed upon the series breaker and not upon a spark gap, and high speed reinsertion is possible since only a single opening action is required.

4.6.1.2 Dual Gap / Non-Linear Resistor Scheme (DGNS)

The above scheme shunts the capacitor with a low impedance path, which although is frequency dependent, its values of inductance and resistance are constant and linear. This results in practically all of the compensating reactance being lost for the by-pass duration. The effect of this is to cause an increase in the effective transfer reactance of the series compensated line section, thereby posing stability and line protection problems. An ideal situation would then be to shunt the capacitor in such a way as to only partially remove the compensating reactance, whilst retaining full protection against overvoltages. This is achieved by inserting a non-linear resistor in series with the dual gap branch to form the dual gap non-linear resistor scheme, DGNS, as shown in Figure 4.6 [54,55].



C - Capacitor bank

D - Damping circuit

G1 - Spark gap , high-set (2.75pu)

G2 - Spark gap, low-set (2.2pu)

B1 - By-pass breaker

B2 - Reinsertion breaker

NR - Non-linear resistor

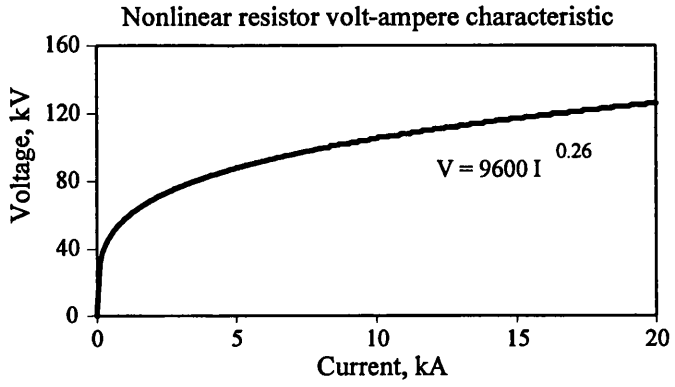


Figure 4.6 Dual gap / non-linear resistor scheme

The impedance in the shunt path varies in sympathy with the voltage developed across the capacitor/resistor combination, producing a self-regulative action, holding the capacitor voltage to an acceptable level, whilst merely reducing the compensation as opposed to losing it altogether with the DGS scheme. However, the by-pass resistor should preferably be non-linear, in order to limit the voltage across the capacitor to a defined level, and to automatically commutate the current back to the capacitor, once the line fault has been cleared. The by-pass non-linear resistor was usually made using Silicon Carbide valve blocks (Varistor). However, due to their insufficient non-linear characteristic, a spark gap and a breaker had to be connected in series with the SiC varistor as shown in Figure 4.6. A back-up spark gap was used to protect the varistor in case of abnormal system faults. The volt-ampere characteristic of the SiC resistor elements used is plotted in Figure 4.6.

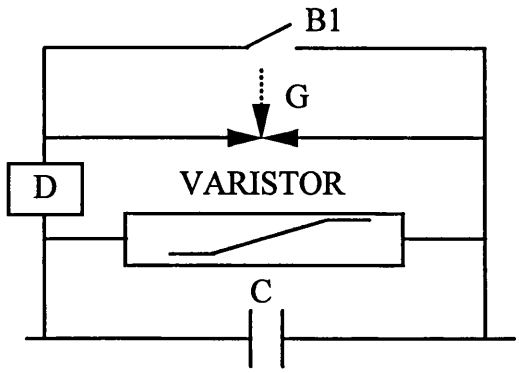
The nonlinear resistor clamps the capacitor voltage below the short-time overvoltage rating during the fault by diverting part of the fault current around the capacitor. With the reduction of capacitor voltage after the fault is cleared, the nonlinear resistor has negligible effect on the magnitude and phase of the capacitor voltage and full compensation is automatically restored immediately after the disturbance, without the need for any breaker switch action at all. The series breaker is then opened some time later to extinguish the gap although the opening delay is no longer critical since very high speed reinsertion has already been achieved. Subsynchronous oscillations that could result from fault clearing are suppressed by the resistor. In addition, the dc offset and reinsertion voltage on the capacitor are eliminated because there is no reinsertion in the conventional sense.

In summary, the inclusion of a non-linear resistor as part of the dual gap branch, introduces the following capacitor protection advantages:

1. Very high speed reinsertion.
2. Improved compensation during the faulted period.
3. Increased damping of subsynchronous current.
4. Reduced voltage peak transient.
5. Reduced stresses on capacitor breakers.

4.6.2 Modern Metal-Oxide Varistor (MOV) Scheme

Advent of the highly non-linear metal oxide (ZnO) varistors for power system applications, have resulted in the development of a new series capacitor protection scheme which is technically more attractive as compared with the foregoing schemes [56,57,58,59]. The MOV protective scheme consists of four basic elements as shown in Figure 4.7. In this case, the varistor is connected directly in parallel with capacitor; the series connected spark gap and breaker can thereby be omitted. The protection is then independent of the action of any spark gaps. A protective level of (2.0-2.5) p.u of the continuous rated capacitor voltage can easily be obtained resulting in a low capacitor cost. A triggered parallel spark gap is needed, however, to protect the varistor during extreme conditions. The gap is designed with an untriggered sparkover voltage higher than the varistor protective level so that the gap will not spark over spontaneously during a fault. Furthermore, the gap is designed so that it will not spark over, even with a triggered impulse, when there is no fault on the line. This eliminates the possibility of gap conduction during normal line operation.



C - Capacitor bank

D - Damping circuit

B1 - By-pass breaker

G - Triggered air gap

Figure 4.7 Metal Oxide varistor protective scheme

The capacitor protection must be modelled in the protection scheme to accurately transfer the voltage across the capacitor. Therefore, it is important to understand the basic principles (including mathematical modelling) of a MOV; these have been summarised in the Appendix A. The basic functions of the MOV scheme are discribed below:

- During the steady state conditions, all power frequency current flows through the series capacitor (negligible current flows in the varistor) and the bypass switch is open and the gap is not conducting.

- Following fault initiation, a high current flowing through the series capacitor results in correspondingly a high voltage across the capacitor and the MOV. The high voltage causes the MOV to conduct excess current, limiting the voltage across it and the series capacitor to the protective level of the varistor. The energy is absorbed by the MOV without closing the by-pass breaker or the trigger gap. Consequently, the capacitor bank is reinserted automatically and immediately upon extinction of the fault current.

- In case the by-pass criteria is fulfilled (a close up fault or a breaker failure), the bank is by-passed by operating the triggered gap and subsequent closure of the by-pass breaker.

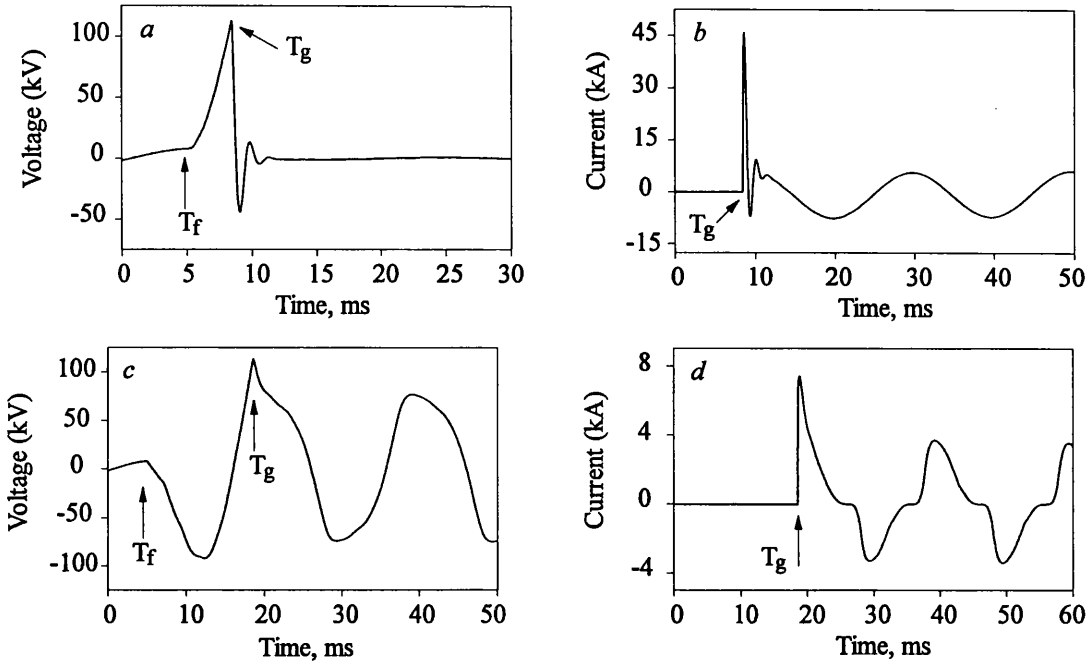
- The MOV acts as the primary overvoltage protector for the capacitor. However, when the duty of the MOV is exceeded due, for example, to the occurrence of extreme system faults, the parallel spark gap is triggered by by-passing the MOV nearly instantly (the firing of this gap is initiated by the control logic that monitors the duty of the MOV). This prevents the energy capability of the resistor from being exceeded. In all other cases, the spark gap will not operate. The breaker B1 also allows an operator to manually insert or bypass the series capacitor. The damping circuit again limits the capacitor discharge current through the gap and/or by-pass breaker.

In summary, the MOV protection provides a number of distinct advantages over the conventional capacitor protection schemes. The main advantage is that it provides quasi-instantaneous insertion thereby maintaining the presence of the capacitor in the circuit at all times. This is important in the case of the unfaulted line. With only gap protection, the unfaulted line would need to have the bypass breaker closed to interrupt conduction of the gaps before the capacitor could be put back into service. In the case of the MOV, when the external fault is cleared and the overvoltage across the capacitor disappears, the MOV stops conducting and the capacitor is back in service. This can result in a substantial increase in power system transient stability and power transfer. The modern MOV scheme eliminates mechanical motion during

the normal protective operation, therefore providing a greater reliability and lower maintenance .

4.6.3 Some Typical Simulation Results Relating to Different Types of Capacitor Protective Schemes

Figure 4.8 illustrates the desirable features of the conventional protective schemes for a typical line to ground fault at the point F1 in Figure 4.2a. Waveforms associated with the capacitor bank closest to the fault are given in Figures 4.8a-d for both DGS and DGNS, from which it is seen that the DGS causes the capacitor voltage to be clamped to almost zero after gap flashover. The DGNS, however, adequately protects the capacitor against overvoltage, whilst maintaining a substantial voltage across the latter. Comparing the by-pass branch current for the two schemes, Figures 4.8b and 4.8d show that for the DGS, the magnitude of the switching transient on gap flashover is considerably higher than that for the DGNS. A direct consequence of these aforementioned very significant differences is that in the case of the DGS, almost complete compensation is removed on gap flashover and remains so until such time as the capacitor has been physically reinserted back into the system. In the case of the DGNS, however, a small degree of compensation (typically about 20% of the prefault steady-state value) is maintained throughout the fault period and this automatically rises to a large value on fault clearance. Although not shown here, it should be mentioned that in the case of the DGS, capacitor reinsertion after fault breakoff is a much bigger step change than for a DGNS, resulting in much larger reinsertion transients in the case of the former.



a Capacitor voltage for DGS *b* Capacitor gap branch current for DGS

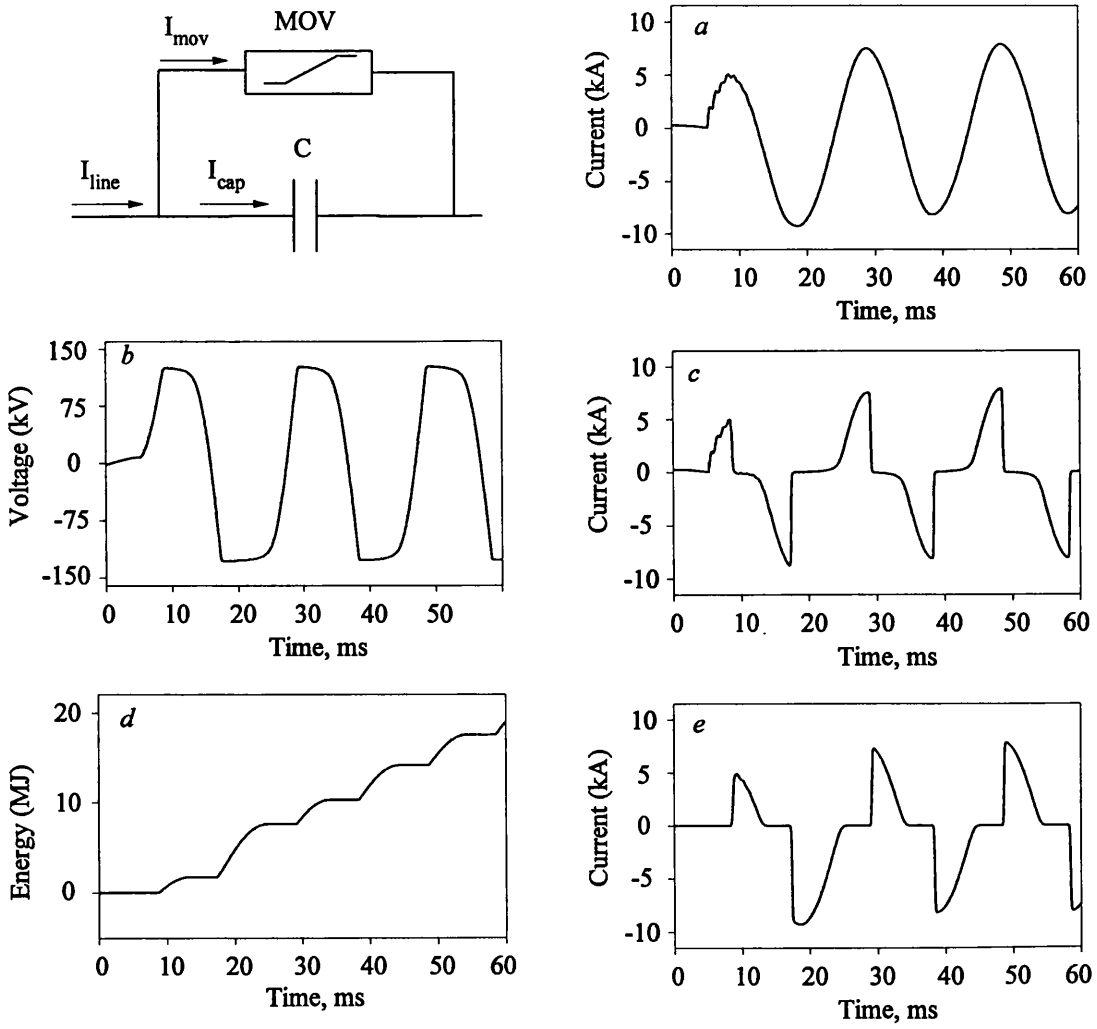
c Capacitor voltage for DGNS *d* Capacitor gap branch current for DGNS

Fault inception, T_f = 5 ms Capacitor gap flashover = T_g

Figure 4.8 Waveforms for conventionl capacitor protective schemes

Figure 4.9 illustrates the EMTP simulated waveforms for varistor voltage, current and energy for a typical line to ground fault at the point F1 in Figure 4.2a. Under normal system conditions, line current flows through the series capacitor and negligible current flows in the varistor. This condition is illustrated in the first quater cycle (5 ms) of waveforms shown in Figure 4.9. A fault occurence on the system increases the capacitor current and voltage. If the capacitor voltage rises enough, the varistor conducts and limits further voltage increase as indicated in Figure 4.9b and 4.9c. The action of the varistor for such a case is illustrated in Figure 4.9d and 4.9e. As can be seen, the varistor limits the voltage on each half cycle and the current alternates between the capacitor and the varistor. When the varistor clamps the voltage, **dv/dt**

is reduced which in turn reduces the capacitor current to a low level. The capacitor/varistor shared conduction continues until the fault is cleared by the system breaker. The line current then drops to the post fault level, reducing capacitor voltage and causing the varistor to virtually cease conduction. Thus the line current flow is fully restored through the series capacitor. This reinsertion is instantaneous and automatic and can markedly increase power system transient stability and power transfer as discussed in the previous sections.



a Line current (I_{line}) *b* Varistor / Capacitor voltage *c* Capacitor current (I_{cap})

d Varistor energy *e* Varistor current (I_{mov}) Fault inception, T_f = 5 ms

Figure 4.9 Waveforms for MOV protective scheme

4.7 Parameters of Series Capacitor Compensation

In this section, the calculated capacitor parameters at power frequency are presented alongwith the calculated threshold voltage for capacitor spark gap operations. As mentioned in section 4.3, basically two series compensated schemes are considered. In the case where two capacitor banks are employed per phase, of the total 70% compensation, 35% is associated with each of the two capacitor banks, whereas in the case of a capacitor bank at the middle of the line, 50% compensation is taken. The value of X_{cap} , the capacitive reactance, used in the representation of the various aforementioned cases is calculated as follows and summarised in Table 4.2.

Positive sequence line reactance (from the Table 4.1) $= 3.03632 \times 10^{-1}\ \Omega$ / km

Total uncompensated circuit reactance $= 3.03632 \times 10^{-1} \times 300$

$= 91.09\ \Omega$

For 70% compensation, capacitor reactance, X_{cap} $= 0.35 \times 91.09$

$= \underline{31.881\ \Omega}$

Table 4.2 Value of capacitive reactance for different level of compensation

Type of scheme	Level of compensation	Capacitor reactance (X_{cap})
Two capacitor banks	Total 70% (35% for each)	63.76 Ω (31.88 Ω)
	Total 50% (25% for each)	45.55 Ω (22.77 Ω)
	Total 30% (15% for each)	27.33 Ω (13.66 Ω)
One capacitor bank	50%	45.55 Ω

4.7.1 Determination of Capacitor Sparkover Voltage

As mentioned in section 4.6.1, the spark gap is set in such a manner that when the voltage across it reaches a certain predetermined threshold value then that particular capacitor is removed from the system. The sparkover voltage is a function of the gap setting and the level of compensation. In the studies presented herein, the sparkover voltage is based on a typical line loading of the 500 kV line of approximately 1 GVA and is calculated as follows and summarised in Table 4.3.

Typical loading of the 500 kV line = 1000 MVA

Full load current, I_{fl} = $1000 \times 10^3 / (\sqrt{3} \times 500)$

= 1.1547 kA

Crest voltage across the each capacitor (for 70%) = $X_{cap} \times I_{fl}$

= 36.813 kV (r.m.s.)

Peak capacitor sparkover voltage, 2.2 p.u, = $2.2 \times 36.813 \times \sqrt{2}$

= 114.53 kV (peak)

Table 4.3 Capacitor sparkover voltages for different level of compensation

Type of scheme	Level of compensation	Sparkover voltage (peak)	
		Gap setting = 2.2 p.u.	Gap setting = 2.75 p.u.
Two capacitor banks	Total 70% (35% for each)	114.53 kV	143.17 kV
One capacitor bank	50%	163.64 kV	204.55 kV

4.8 Summary

In summary, the system simulation of the power system has been done using the EMTP software. It is vitally important that the system simulation be as accurate as possible within the bounds of practicality. In this respect, the various types of independent protection equipment associated with the series capacitor banks must be modelled in the protection scheme to accurately transfer the voltage across the capacitor. Great attention is focused upon the modelling of the MOV which forms an integral part of most modern capacitor protection units.

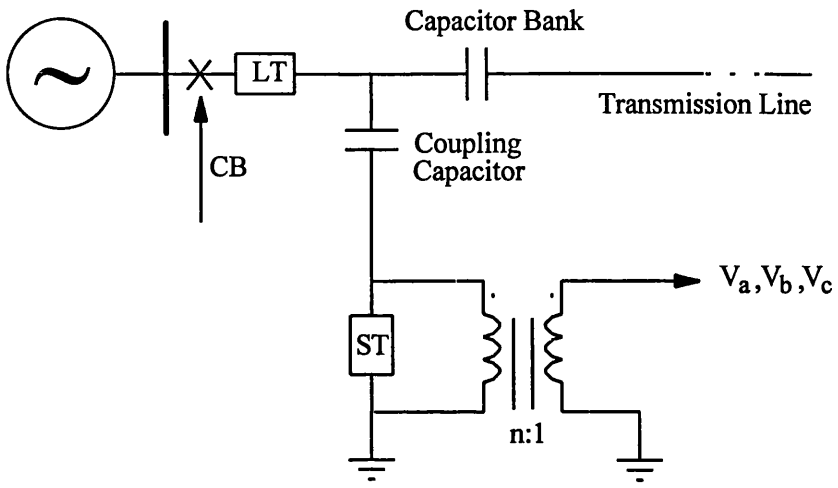
CHAPTER 5

RELAY STRUCTURE

5.1 Introduction

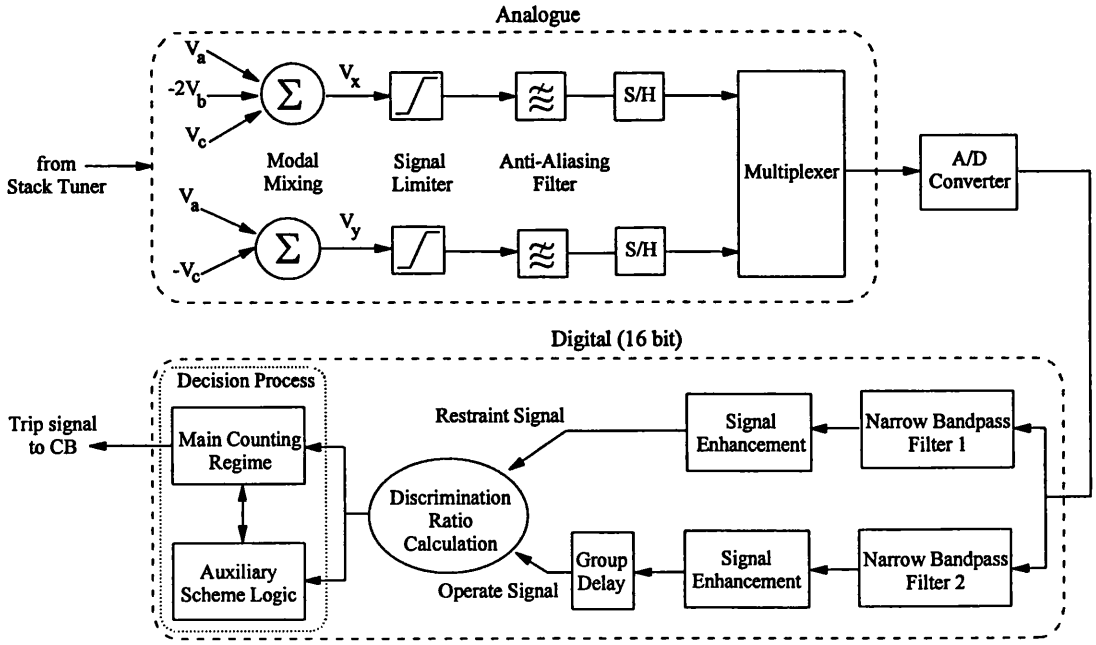
This chapter describes the individual components that make up the new protection system and their implementation. The block diagram of the full protection system from the primary system to the relay outputs is shown in Figure 5.1a and 5.1b respectively. All of the operations are performed on the measured signals at each end of the circuit to give the locally derived trip decisions.The new relay scheme is designed for implementation with the latest generation of high performance digital hardware comprising a 16-bit A/D converter. In this respect, it should be mentioned that the although latter gives a high resolution, some signal limitation is necessary in order to cope with the large dynamic range associated with fault generated HF signals. The outputs from the stack tuners are thus first stepped down by an auxiliary transformer as shown in Figure 5.1a. In practice, this comprises of a specially designed low-loss core which has a very wide bandwidth capable of passing high frequency components with little attenuation. The scaled-down stack tuner outputs

are then passed to the special designed signal processing unit as shown in Figure 5.1b. The basic signal processing arrangement comprises analogue and digital circuits and details of each of the processes are explained below.



LT = line trap, ST = stack tuner, CB = circuit breaker

(a) Primary system



(b) Basic signal processing units

Figure 5.1 Block schematic diagram of the complete protection scheme

5.2 Analogue Signal Processing

This basically comprises a signal mixing circuit, a signal limiter, an anti-aliasing filter and an analogue to digital converter as shown in Figure 5.1b. In this part, the output signals of the stack tuner corresponding to three phase voltages V_a, V_b, V_c are combined in both aerial mode 2 (1,-2,1) and mode 3 (-1,0,1) to form the composite signals V_x and V_y for detection of various types of fault. The signal outputs from the modal mixing circuit are then passed through a limiter; an anti-aliasing filter is employed in order to minimise errors arising due to aliasing of high frequency signals above the Nyquist frequency of 100 kHz before the signals are digitised through an A/D converter.

5.2.1 Modal Mixing Circuit

The output of each stack tuner is combined to form a composite signal in such a way as to cover all faults encountered in practice. In the relay technique described here, the modal-transformation method [26,60] is employed to decouple the phase signals into their respective modes. A distributed parameter three phase transmission line can be described by the following differential equations:

$$\frac{dV}{dx} = -ZI \quad ; \quad \frac{dI}{dx} = -YV \tag{5.1}$$

where **V** and **I** are column matrices corresponding to the voltages and currents of each phase,

$$V = \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad ; \quad I = \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \tag{5.2}$$

Z is the line impedance matrix and **Y** is the line admittance matrix.

Then

$$\frac{d^2V}{dx^2} = -Z\frac{dI}{dx} = ZYV = PV \tag{5.3}$$

and similarly

$$\frac{d^2I}{dx^2} = YZI = P^TI \tag{5.4}$$

The matrix solution is based on a linear transformation of voltages and subsequent manipulation, so that second-order differential relationships involve diagonal matrices only. Mutual effects are thus eliminated, making a direct solution components for component possible.

Modal component-voltage matrix $\mathbf{V^C}$ is introduced, related to phase-voltage matrix by

$$V = SV^C \tag{5.5}$$

Substitution in Equation 5.3 and rearrangement yields

$$\frac{d^2}{dx^2}(SV^C) = PV = PSV^C \tag{5.6}$$

$$\frac{d^2V^C}{dx^2} = S^{-1}PSV^C \tag{5.7}$$

Matrix **S** is chosen in such a way that $\mathbf{S^{-1}PS}$ is a diagonal matrix and so **S** is a matrix

of Eigenvectors of **P**. These modal components are, therefore, independent of other components and the Eigenvalues of **P** are the *Modal propagation constants*. The components of $\mathbf{V}^C$ are associated with the *natural modes of wave propagation* and **S** is the *Modal voltage matrix.*

Essentially, the phase variations of currents are transformed as indicated in Equation 5.8 and 5.9.

$$I = QI^C \tag{5.8}$$

$$\frac{d^2I^C}{dx^C} = Q^{-1}P^TQI^C \tag{5.9}$$

Again, $\mathbf{Q^{-1}P^TQ}$ is arranged to be diagonal and Q is the *Modal current matrix.*

There are a number of different transformation matrices (**Q** and **S**) which can be chosen to diagonalise the products $\mathbf{S^{-1}PS}$ and $\mathbf{Q^{-1}P^TQ}$. If an ideally transposed single-circuit line is considered, the form **Q=S** given in Equation 5.10 (the *Clark's* transformation) is particularly useful in that, the modal components of voltage and current are easily derived as linear scalar combinations of the actual phase variations.

$$Q = S = \begin{bmatrix} 1 & 1 & 1 \\ 1 & 0 & -2 \\ 1 & -1 & 1 \end{bmatrix} \tag{5.10}$$

Since

$$V^C = S^{-1}V \tag{5.11}$$

$$\begin{bmatrix} V^{C1} \\ V^{C2} \\ V^{C3} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ \frac{3}{2} & 0 & -\frac{3}{2} \\ \frac{1}{2} & -1 & \frac{1}{2} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_C \end{bmatrix} \qquad (5.12)$$

The behaviour of any uniform line can be divided into a number of independent modes of propagation. In general $\mathbf{S} \neq \mathbf{Q}$, so the voltage and current distribution in the same mode will be different. Only the voltage are of interest in this work and so any changes to modal current distribution caused by the amount of line transposition for example, are not of any interest. Only the two aerial modes are required and they can be simplified to:

$$V_x = V^{C2'} = V_a - 2V_b + V_c \quad \rightarrow \quad mode\ 2 \qquad (5.13)$$

and

$$V_y = V^{C3'} = V_a - V_c \quad \rightarrow \quad mode\ 3 \qquad (5.14)$$

where V_x, V_y, $V^{C2'}$ and $V^{C3'}$ are the aerial mode voltages and V_a, V_b and V_c are the phase voltages. It can be shown that aerial mode signal based on the mode-2 combination satisfactorily covers all earth faults and pure phase faults except pure phase fault involving phases 'a' and 'c'. The latter is, however, covered by the mode-3 signal.

With this approach, any common-mode signals (due to mutual coupling) induced in the line which result, for example, from adjacent parallel line and/or multiple circuits sharing the same right of way are eliminated; this is so because such spurious signals principally associated with earth mode signals are not employed in this technique. This ensures immunity to all disturbances other than those associated with the line

to which the protection equipment is connected. This would also be true in situations where parallel lines have line traps tuned to different centre frequencies.

5.2.2 Signal Limiting and Analogue Pre-Filter

The two modal signals have a large dynamic range. For example, for faults occurring near voltage maximum, there is a very large initial burst of HF signals of several kilovolts, predominantly due to the presence of very significant travelling wave components that are associated with such faults. The net effect of this is that, at least during the initial very short period following a fault, the bursts of HF signals associated with the nonlinear behaviour of the fault arc current get swamped by the very dominant travelling wave components. Conversely for faults near voltage zero, the travelling wave components are virtually nonexistent and the bursts of HF signals are predominantly due to the distortion caused by the nonlinear arcing fault. These signals normally only have a magnitude of several volts.

Although a 16 bit A/D conversion process is employed and it gives a high resolution, it is difficult to accommodate the complete range of signal level. This means that in order to retain relay sensitivity for a large majority of practically encountered faults, including low level faults, it is necessary to reduce the dynamic range of the relay. This is achieved by passing the analogue HF signals through a signal limiter to clip them (particularly those associated with the aforementioned very large initial bursts) to the required level. In this respect, the clipping level and the turns ratio of the auxiliary step down transformer connected to the stack tuner output has to be

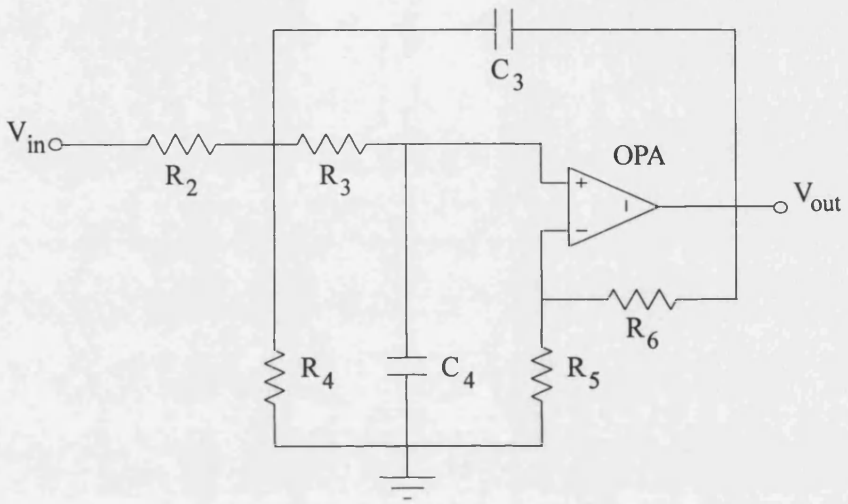
carefully chosen to ensure that the minimum levels of fault signals likely to be encountered in practice are always well above the background noise level (which are discussed in section 5.2.3) admitted into the relay. In practice, the auxiliary transformer is a specially designed wideband device which has a radio-metal core and a turns ratio of 200:1. An extensive series of CAD studies have shown that this ratio adequately covers the requisite dynamic range.

The scaled-down phase signals from the secondary of the auxiliary transformer are limited to ±10V directly after being combined to form the two modal signals. The signals are then passed through a second order Butterworth anti-aliasing filter with a cutoff frequency of approximately half the digital sampling frequency of 200 kHz before being inputted into the A/D convertor. In this respect, it should be noted that in practice, the fault generated noise signals contain HF components over a wide bandwidth, with little attenuation of signals up to about 500 kHz. There is thus a need to actively remove any frequency components which are greater than half the sampling frequency in order to minimise any errors arising due to signal aliasing. The Butterworth filter is employed as it is commonly used for anti-aliasing in circuits that sample analog waveforms because it transmits signal amplitudes faithfully [61].

The filter is implemented using a Sallen-Key circuit as shown in Figure 5.2, having the transfer function:

$$H(S) = \frac{2.7435\times10^{11}}{S^2+740740S+2.7435\times10^{11}} \qquad (5.15)$$

The frequency response of the filter is given in Figure 5.3. All of the analogue emulations, such as the signal limiting, modal mixing and anti-alias filtering, were performed within the EMTP software.



$R_2 = R_3 = R_6 = 270\Omega$; $R_4 = R_5 = 1.1k$; $C_3 = C_4 = 10nF$; OPA = AD841

Figure 5.2 Circuit diagram of anti-aliasing filter

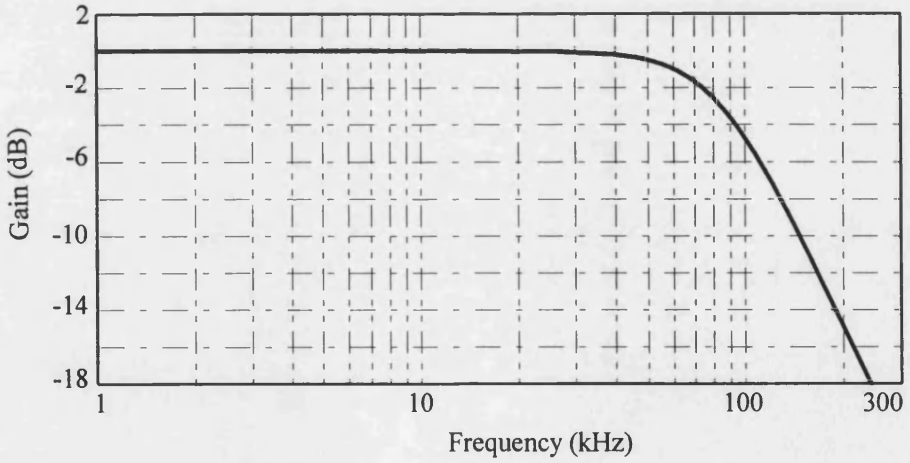


Figure 5.3 Frequency response of anti-aliasing filter

5.2.3 Analogue to Digital Conversion and Practical Noise Consideration

The necessary resolution for converting a ±10 V analogue signal into digital form is achieved by a 16 bit A/D converter. This corresponds to 2^{15} or 32768 quantum levels representing the 10 V input. In practice, there can be spurious HF noise present on the system. This can be due to a number of factors such as corona discharge, thermal agitation of conductors, electromagnetic interference, etc. High voltage laboratory tests [62] and practical experience has shown that the maximum level of background noise likely to be admitted into the front end of the relay is typically about 20 mV. This corresponds to a digital level of 65 quanta for the ±10 V, 16 bit A/D converter. A threshold set at this level within the relay algorithm thus ensures that the relay is stable under healthy conditions, without its sensitivity being unduly affected for internal faults.

5.3 Digital Signal Processing

The digital signal processing part comprises of essentially digital filters, signal enhancement and a decision process as shown in Figure 5.1b. In practice, this processing would be carried out within a high performance floating point processor. The operate and restraint quantities are calculated for both of the modes and so two discrimination ratios are calculated within each relay.

5.3.1 Digital Filtering

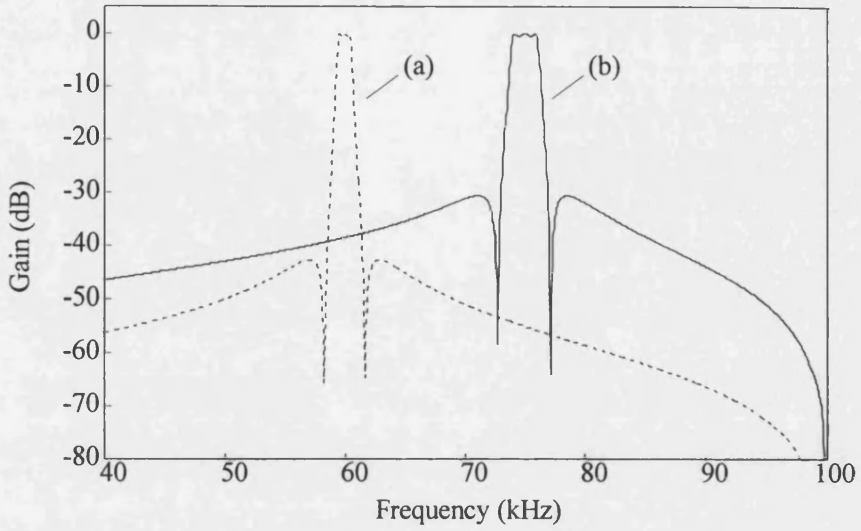
For the protection technique described here, it is necessary to process the HF signals through two bandpass filters with quite narrow bandwidths and fairly sharp cutoff frequencies. Sixth order elliptic infinite impulse response (IIR) filters are used as they give a very rapid transition between stop and pass bands, with a minimum filter order, and therefore, minimum group delay [63]. The choice of the filter centre frequencies is crucial to the correct operation of this protection scheme. However, the centre frequency choice mainly depends on the practical hardware available, particularly in terms of processing power and speed.

The *operate* filter frequency is fixed by the centre frequency of the line trap, in this case 75 kHz. The *restraint* filter frequency is chosen through an extensive series of studies for optimal relay performance. These studies involved examining the small drifts in the tuned centre frequency of the line trap resulting from a variation in the line trap parameters caused by environmental factors. For the application considered here, a 2 kHz bandwidth filter was used at the operate centre frequency of 75 kHz and a 1 kHz bandwidth filter at the restraint centre frequency of 60 kHz. The Z-domain filter transfer functions are of the form shown in Equation 5.16 and their frequency responses are shown in Figure 5.4.

$$H(Z) = C \prod_{k=1}^{3} \frac{1 + a_{1k} Z^{-1} + a_{2k} Z^{-2}}{1 + b_{1k} Z^{-1} + b_{2k} Z^{-2}} \tag{5.16}$$

where a_{nk} and b_{nk} are the individual filter coefficients and these are summarised in Table 5.1. The risk of filter instability was minimised by implementing the filters

using cascaded second order sections.



(a) Restraint filter (b) Operate filter

Figure 5.4 Digital filter frequency response

Table 5.1 Digital filter coefficients

Restraint filter				Operate filter			
C = 0.00098912904				C = 0.0049238537			
a_{11}	0	b_{11}	0.61183411	a_{11}	0	b_{11}	1.3846364
a_{21}	-1	b_{21}	0.97969252	a_{21}	-1	b_{21}	0.95720547
a_{12}	0.5143319	b_{12}	0.58448660	a_{12}	1.3094460	b_{12}	1.3555679
a_{22}	1	b_{22}	0.99074483	a_{22}	1	b_{22}	0.98285133
a_{13}	0.71833336	b_{13}	0.64557229	a_{13}	1.5066711	b_{13}	1.4477929
a_{23}	1	b_{23}	0.99084115	a_{23}	1	b_{23}	0.98392612

5.3.2 Signal Enhancement

As outlined in reference 35, the two discriminant signals attained via the above mentioned digital filters can be greatly enhanced by integrating the square of the signals. This effectively gives a measure of the spectral power content of each signal, thereby allowing a better comparison to be made. The mean power, P_m of a continuous signal $x(t)$ can be measured using Equation 5.17 [64].

$$P_m = \frac{1}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} x^2(t)\,dt \tag{5.17}$$

where $x(t)$ is a continuous time signal and **T** is period. Since the signals being dealt with are in the digital domain (discrete time signals), the integral is replaced with a summation. The bandpass filter outputs are first squared and then averaged over a 1.25 ms (250 sample) long moving window as shown in Equation 5.18 to give a measure of their spectral power.

$$V_z(n\Delta t) = \sum_{k=n-L}^{n} \frac{V_f^2(k\Delta t)}{L} \tag{5.18}$$

where $V_z(n\Delta t)$ is the enhanced output at time $n\Delta t$, n is the time step number, Δt is the time step length (sampling interval), V_f is the bandpass filter output and L is the length of moving average window (250 samples = 1.25 ms at the 200 kHz sampling rate). It is assumed that a high performance processor with floating point arithmetic would be used in the hardware implementation of the relay design. This removes the need to use scaling factors to avoid arithmetic overflow problems.

5.3.3 Discrimination Ratio Calculation

It should be noted that since the two IIR filters are designed around different centre frequencies, there is a small difference in their group delays. Thus the operate signal has to be delayed by 40 samples to equalise them and so eliminate any phase shift errors. The discrimination ratio is calculated from the ratio of the enhanced operate filter output to the enhanced restraint filter output and the former determines whether a fault is internal or external. For internal faults, this ratio will be equal to or greater than unity, whereas it will be very close to zero for external faults. The latter is so by virtue of the fact that for an external fault, there is heavy attenuation of the signal level at the centre frequency of 75 kHz thereby significantly affecting the magnitude of the operate signal.

5.3.4 Decision Process

A specially designed decision process has also been incorporated into the relay algorithm for each of the modes, to improve the relay security. It comprises a counter whose value is incremented or decremented according to the value of discrimination ratio. When either of the trip counters exceed a preset threshold level, an output to trip the local circuit breaker would be initiated.

5.3.4.1 The Counting Regime

Extensive CAD studies were carried out to ascertain the optimum setting of the counting regime and trip threshold level. These studies involved simulating a wide

range of fault conditions and then calculating the filter responses and discrimination ratios. The decision logic was then applied to these results and the performance of different counting regimes and threshold levels was assessed. The main counting regime that was decided upon is summarised in Table 5.2. As can be seen, when the discrimination ratio (d) is close to or above unity, the counter is incremented rapidly as the ratio gives a strong indication of an internal fault. When the ratio is between 0.8 and 0.4, the counter is incremented more slowly as there is some degree of uncertainty about the presence of an internal fault. The counter is decremented slowly, when the ratio falls below 0.4. The counter is decremented rapidly when the ratio is close to zero as this gives a strong indication of an external fault. However, its value is never allowed to fall below zero.

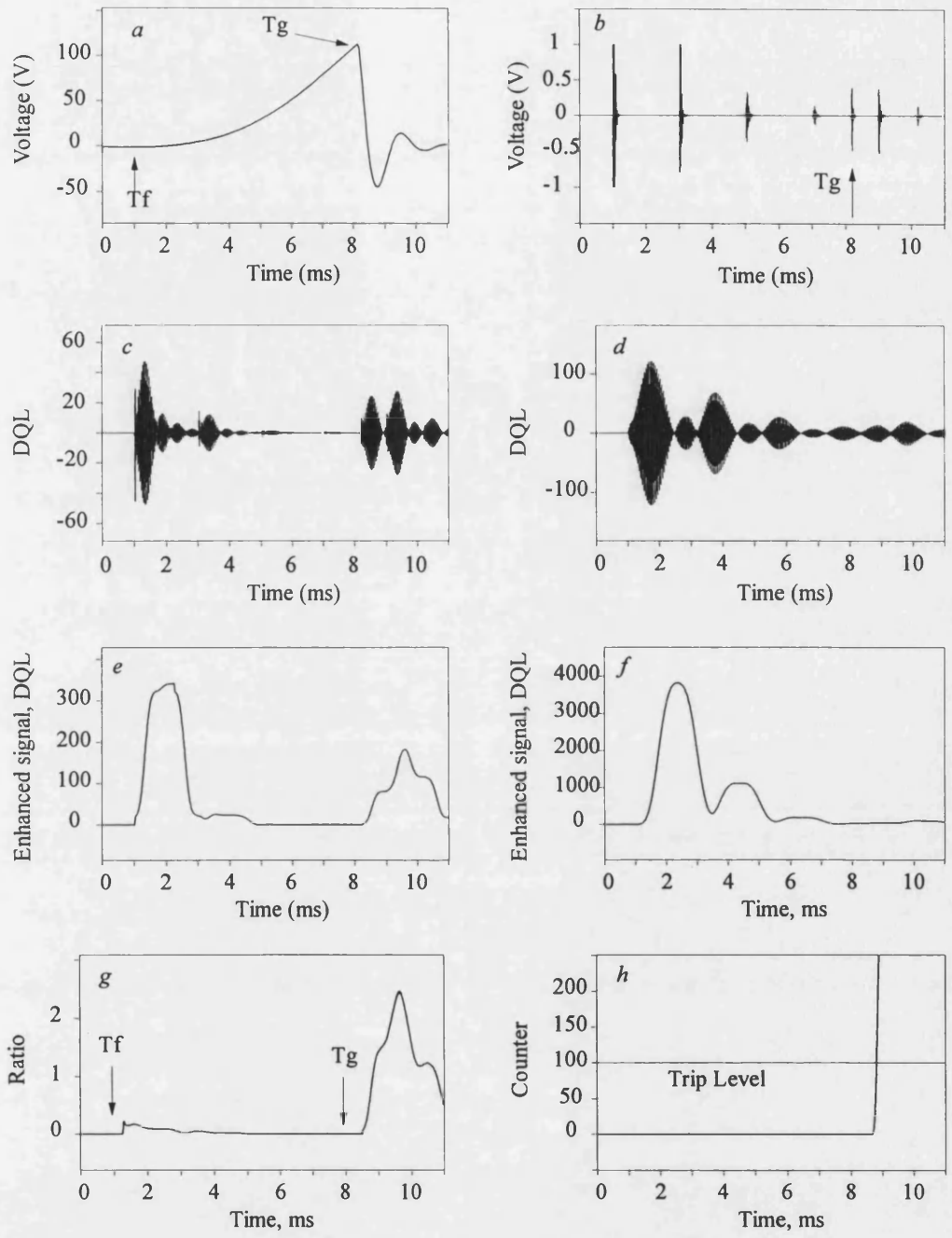
Table 5.2 The decision logic

Discrimination ratio, d	Counter increment
$d \geq 1.0$	+10
$1.0 > d \geq 0.8$	+8
$0.8 > d \geq 0.6$	+4
$0.6 > d \geq 0.4$	+1
$0.4 > d \geq 0.2$	-1
$0.2 > d \geq 0.1$	-4
$0.1 > d \geq 0.01$	-8
$0.01 > d$	-10

5.3.4.2 Auxiliary Scheme Logic

It should be noted that, unlike with plain feeders, in series compensated lines there can be present some spurious HF noise in the relaying signals, in addition to the noise generated by genuine arcing faults, and this is as a direct result of the operation of the capacitor protective gaps, which is very random in nature. Whilst this is of no consequence for internal faults since any additional HF noise arising from capacitor gap flashover actually enhances relay performance by augmenting the signals, it can threaten relay stability of a healthy circuit for an external fault. This situation is clearly shown in Figure 5.5.

Figure 5.5 shows the relay response to an 'a'-earth external fault near voltage zero of the 'a' phase voltage, immediately behind the line trap and on the busbar at the end S (at F_8 at Figure 4.2b). In this particular fault study, DGS is employed and the 'a' phase capacitor gap at end S flashover in approximately 7ms after fault (see Figure 5.5a). Considering the time domain response of the composite signal at end S (Figure 5.5b), the additional bursts of HF noise generated on gap flashover are evident. As excepted for this external fault, the signal detected by the operate filter is less than that measured at the lower restraint frequency (Figures 5.5c-d). However, the effect of the gap flashover on the signals at each stage of the digital signal processing unit is clearly seen from Figures 5.5c-h. The discrimination ratio rises above 'one' after gap flashover (ie. 7ms after fault inception), causing the trip counter to exceed the trip level. Therefore, the relay issues an unwanted trip decision for this external fault.



a Capacitor voltage waveform

b Mode 2 analog signal

c Operate filter output

d Restraint filter output

e Enhanced operate filter output

f Enhanced restraint filter output

g Discrimination ratio

h Counter output

Fault inception, T_f = 1 ms Capacitor gap flashover = T_g

DQL = Digital quantum levels

Figure 5.5 Mode 2 relay response with DGS for an external voltage zero fault

Thus apart from the aforementioned counting regime, there is a concomitant requirement to build into the decision process an auxiliary scheme logic. In this respect, an extensive series of studies have revealed that there is always a significant time lapse ($\geq$ 5 ms) between the occurrence of an external fault and any gap flashover on a healthy circuit. In the relay scheme described herein, the problem of possible relay instability has thus been overcome by simply monitoring the behaviour of the decision counter in a small window length w_p following a fault. If it stays well below the trip level over the entire period associated with this window, the fault is assumed to be external and the counter is simply set to zero and not allowed to increase thereafter. A flow diagram of decision process and a auxiliary scheme logic, showing their operation, are shown in Figures 5.6 and 5.7, respectively.

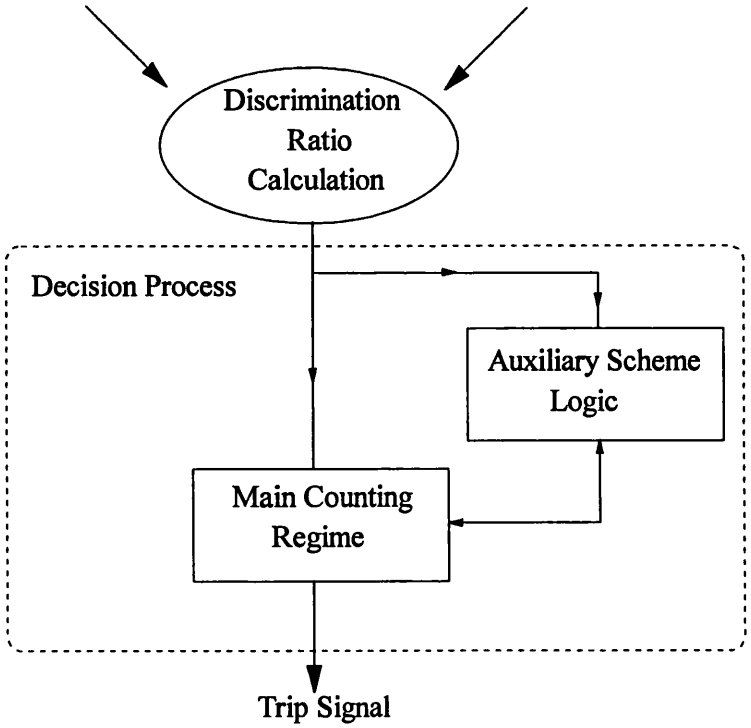
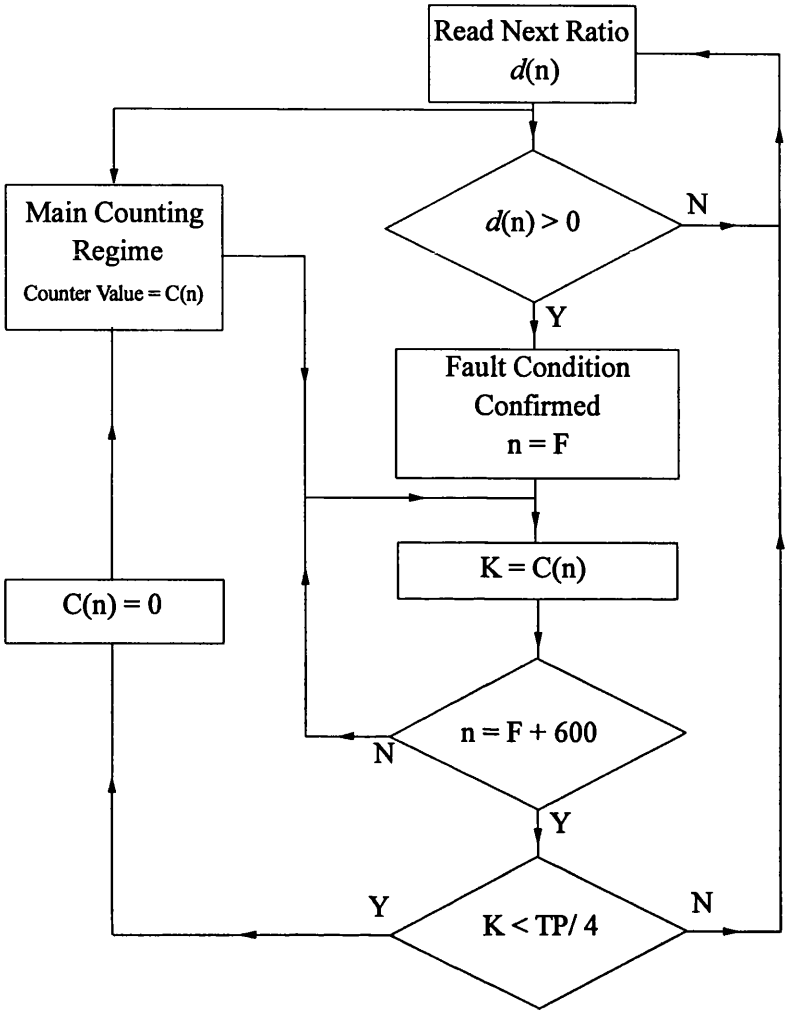


Figure 5.6 Decision process



d(n) = discrimination ratio C(n) = counter value

TP = trip level

Figure 5.7 Auxiliary scheme logic algorithm

Extensive CAD studies were carried out to ascertain the optimum settings of the decision and trip level. As shown in flow diagram in Figure 5.7, for the relay described here, the above mentioned fixed window length w_p set to 600 samples (3 ms) and a trip level of 100 have been found to give a rapid relay trip for internal faults whilst the counter remains well below this level and restraints for external faults.

Figure 5.8 shows the counter output with auxiliary scheme logic for aforementioned fault conditions. As shown in Figure 5.4g, more importantly, the discrimination ratio stays well below unity for a significant time period after fault inception and as a consequence, the auxiliary scheme logic within the decision process recognises this as an external fault and inhibits any increment in the counter output once the pre-defined time window of 3ms has been surpassed; this is evident from Figure 5.8.

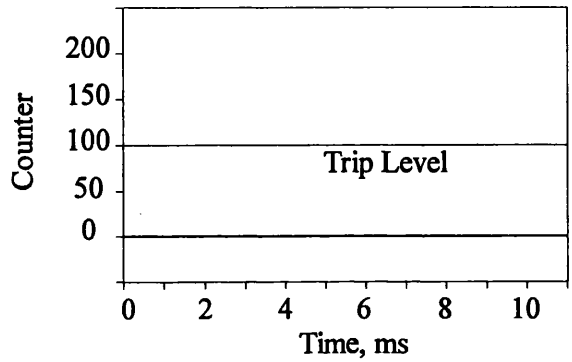


Figure 5.8 Counter output for an external fault with auxiliary scheme logic

A decision process of this nature thus provides a near optimum performance in which the relay retains its maximum sensitivity in the initial fault detection period (particularly for internal faults) and any relay mal-operation is prevented from occurring for the external fault during the entire period that the signals become significantly finite after capacitor gap(s) flashover. It should be mentioned that the auxiliary scheme logic based on a window length w_p=3 ms has no detrimental effect on relay performance for internal faults.

For the work presented in this thesis, all of the digital signal processing, ie the A/D

conversion through to the trip output, has been implemented using off-line computer programs written in Microsoft Fortran 77. Therefore, no delays due to the analogue processing and the finite amount of time the processor takes to perform the calculations, etc, are taken into account. It is envisaged that the relay calculation will be performed using four Texas Instruments TMS320C40 floating point parallel processors which are specially designed for digital signal processing at very high sample rates and are capable of performing 275 million operations per second. In this respect, although in practice there would be some delays within the data acquisition system and processor calculation delays, thereby adding to the relay operating time, it is estimated that the overall tripping times of output would still be less than five milliseconds after fault inception.

5.4 Summary

The new protection relay structure and CAD techniques including emulation of analogue interface and hardware are explained in great detail. Particular attention is given to the filtering process employed in the relay. In the analogue part of the relay, the design of the anti-aliasing filter and in the digital section the design of the two narrow band filters are thoroughly discussed. The design and performance of a special decision process within the relay algorithm is finally explained. More importantly, it has been developed to satisfactorily deal with the protection problems commonly encountered in series compensated lines.

CHAPTER 6

RELAY PERFORMANCE FOR THE SYSTEMS WITH MOV CAPACITOR PROTECTIVE SCHEMES

6.1 Introduction

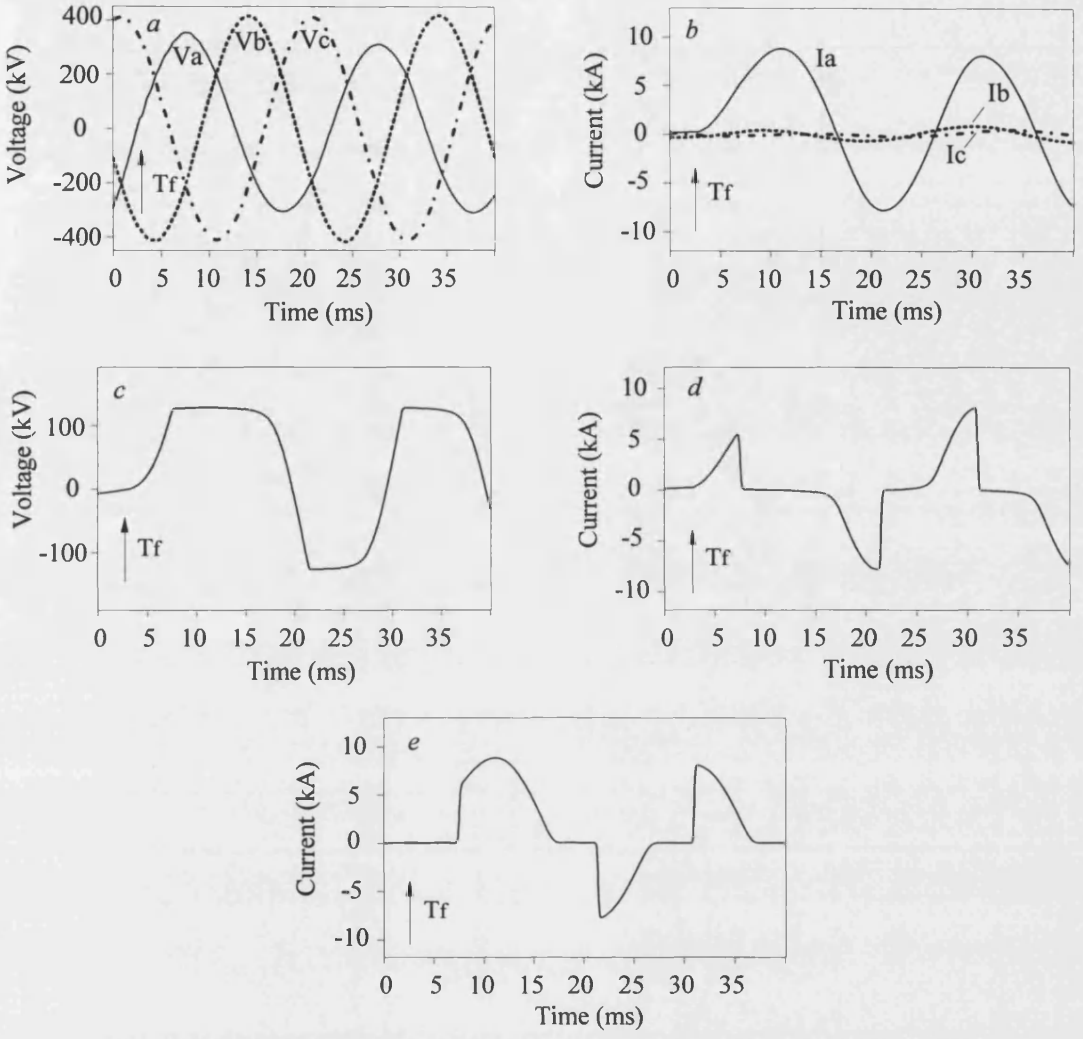
This chapter describes the performance of the new protection relay for a variety of practically encountered fault conditions on series compensated power systems particularly when the MOV capacitor protective scheme is employed. The different network configurations studied have already been explained in some detail in section 4.3. Briefly, as shown in Figure 4.2a-d, line S-R represents the series compensated main line; 'End S' represents the busbar closest to the sending end relay while 'End R' represents the busbar closest to the receiving end relay. The fault positions and their respective distances from the busbar are clearly indicated on each diagram. Greater emphasis is placed on the relay performance for single phase to earth faults in this thesis as these are by far the most common faults encountered in practice.

6.2 Typical Internal Fault Response

In order to fully appreciate the measuring technique implemented and the operation of the relay scheme, it is useful to examine the outputs of different relay stages for a typical fault condition. Figure 6.1 typifies the waveforms for an internal 'a'-phase to earth fault applied 2.5 ms after time zero, close to voltage zero and 80 km from end S, ie. at F_1, on the network of Figure 4.2a.

First of all, considering the primary system voltage waveforms at end S, Figure 6.1a shows a reduction in the faulted phase voltage (in comparison to the healthy phase voltages) with very few transients as the fault is applied close to voltage zero. The typical dc offset on the current waveform associated with voltage zero faults is shown in Figure 6.1b. As expected, the faulted phase current magnitude is significantly greater than the unfaulted phase currents.

The behaviour of the MOV for this fault condition is illustrated in Figures 6.1c-e; as expected, both the capacitor current and voltage increase on fault inception. Once the capacitor voltage rises above a certain level, the MOV conducts and limits further voltage increase. This voltage is limited on each half cycle and the current alternates between the capacitor and the varistor. The capacitor/MOV shared conduction continues until the fault is cleared by the opening of the main line circuit breakers.



a End S phase voltages

b End S phase currents

c End S a-phase capacitor voltage

d End S a-phase capacitor current

e End S MOV / bypass current

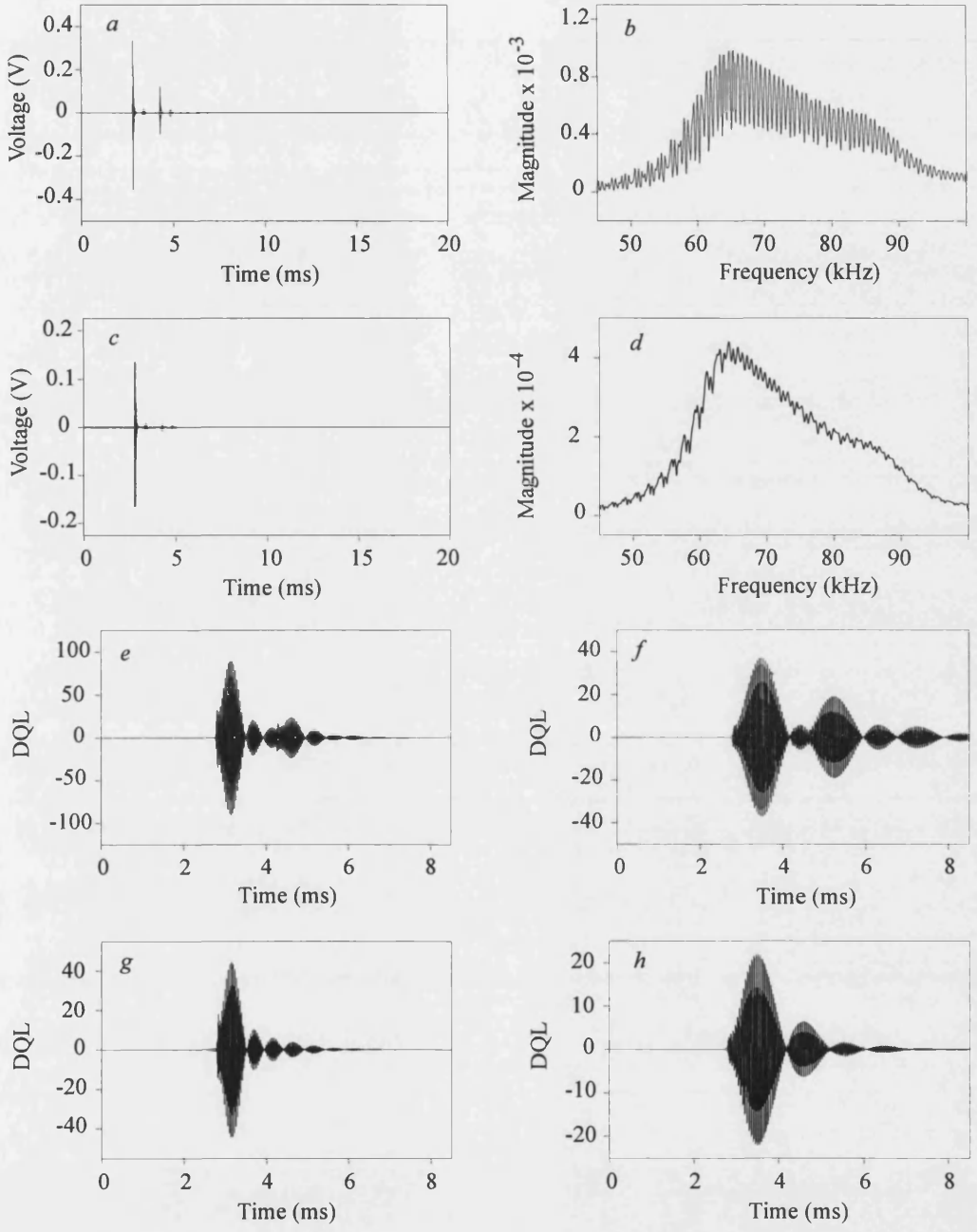
Fault inception, T_f = 2.5 ms

Figure 6.1 Typical internal faulted phase voltage and current

Figures 6.2 and 6.3 depict the behaviour of the various signals (based on the two aerial modes 'x' and 'y') within the digital processing hardware (as defined in equations 5.13 and 5.14). The stack tuners are specifically designed to capture the HF disturbances generated by the arcing faults. The stack tuner outputs at end S contains

a number of different bursts as evident from Figures 6.2a, c. The initial burst is at fault inception and the other subsequent bursts are due to fault arc restrikes. As the fault is internal to the protected zone, the HF signals are little affected by the line traps ie., there is no attenuation of either mode around the centre frequency of 75 kHz (Figures 6.2b, d). The narrow bandpass digital filters associated with both modes, therefore, detect signals of a fairly similar strength (Figures 6.2 e-h). After spectral power enhancements of the signals, the operate signals are significantly higher than the corresponding restraint signals (Figures 6.3a-d). Thus the discrimination ratios associated with both modes 2 and 3 are well above unity for this internal fault.

When considering the function of the decision process, Figures 6.3f, h clearly show that for this internal fault, the decision counters quickly attain the requisite trip level and issue trip decisions in approximately 0.6 ms after fault inception. It should be mentioned that these tripping times do not take into account any delays due, for example, to the data processing times. In practice these are likely to add a few milliseconds (typically 3 ms) to the overall relay operating times.



a Mode 2 analogue signal

b Frequency spectrum of *a*

c Mode 3 analogue signal

d Frequency spectrum of *c*

e Mode 2 operate filter ouput

f Mode 2 restraint filter output

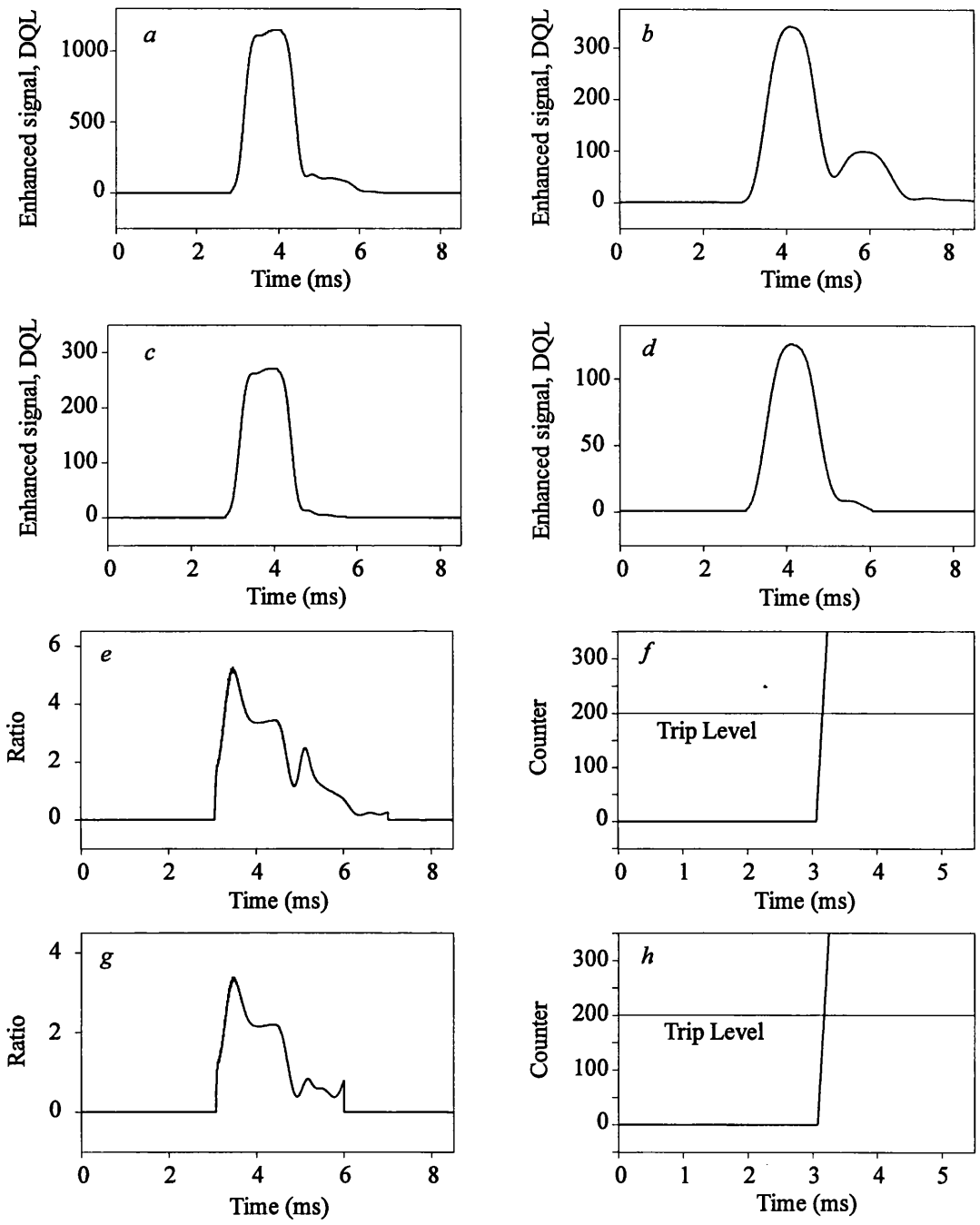
g Mode 3 operate filter output

h Mode 3 restraint filter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 6.2 Typical internal fault response



a Mode 2 enhanced operate filter output *b* Mode 2 enhanced restraint filter output

c Mode 3 enhanced operate filter output *d* Mode 3 enhanced restraint filter output

e Mode 2 discrimination ratio *f* Mode 2 trip counter output

g Mode 3 discrimination ratio *h* Mode 3 trip counter output

Fault inception, T_f = 2.5 ms

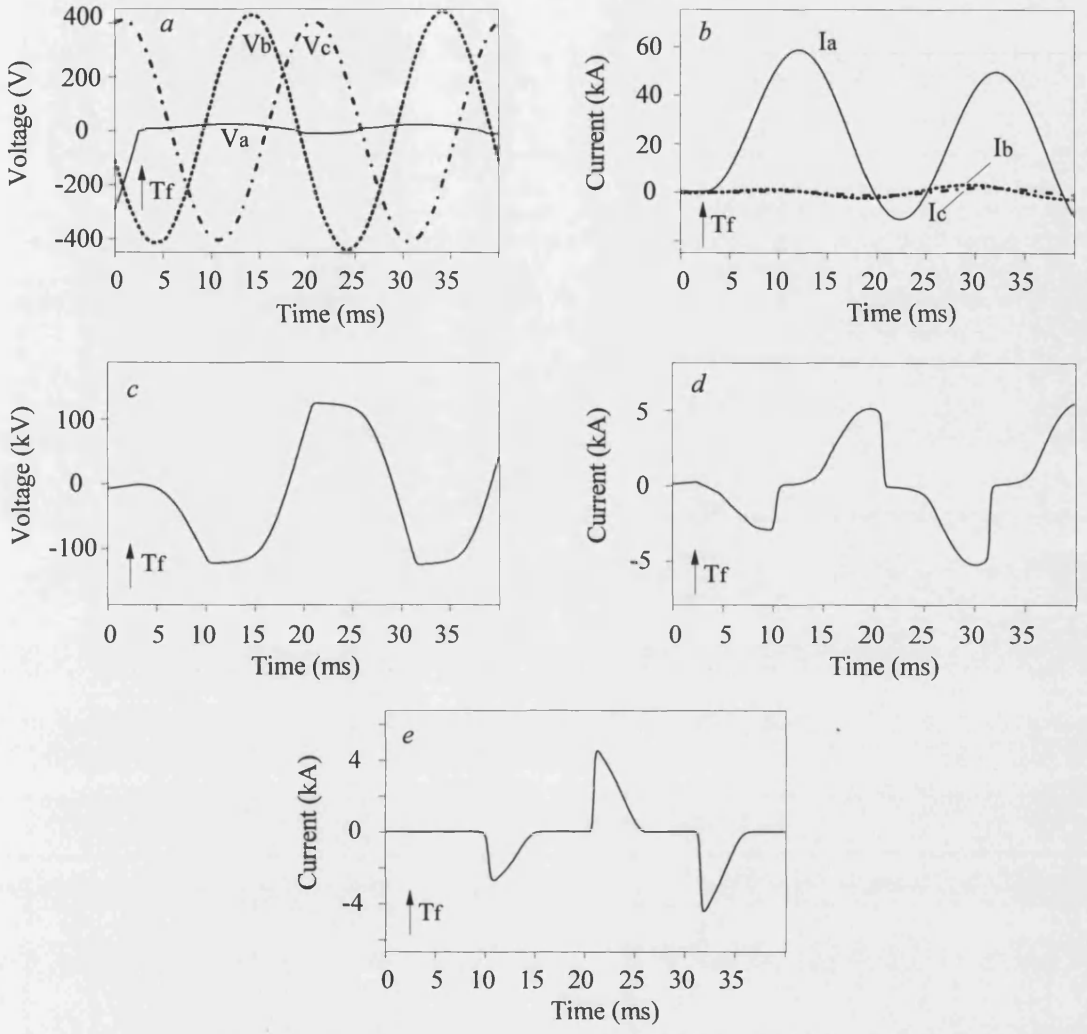
DQL = Digital quantum levels

Figure 6.3 Typical internal fault response

6.3 Typical External Fault Response

A similar fault ie. an 'a'-phase to earth fault near voltage zero, is applied on the busbar at end S, just behind the line trap, to create an external fault response (at F_2 in Figure 4.2a) and again MOV capacitor protective scheme is employed. As shown in Figure 6.4a, the faulted phase voltage collapses to near zero when the fault is applied (after 2.5 ms) and this is due to the fault point being very close to the busbar; the subsequent voltage is essentially due to the small fault arc resistance. The faulted phase current is again almost fully offset as the fault inception angle is very close to zero (Figure 6.4b). The behaviour of the MOV for this external fault is illustrated in Figures 6.4c-e.

As shown in Figure 6.5a and c, the time domain responses of two composite signals at end S appear to be very similar to the internal fault case. However, in the frequency domain, the blocking effect on the narrow band of frequencies around 75 kHz can be clearly seen from Figures 6.5b and d. The signals detected by the operate filters are, therefore, significantly less than those associated with the restraint filters (Figures 6.5e-h). As expected, the spectral energy content of the restraint signals is considerably greater than that of the operate signals as evident from the corresponding enhanced filter outputs of Figures 6.6a-d. The discrimination ratios peak at about 0.12 very shortly after fault inception (Figures 6.6e, g), and as these are well below unity, the counter outputs remain at zero and hence no trip decisions are asserted (Figures 6.6f, h).



a End S phase voltages

b End S phase currents

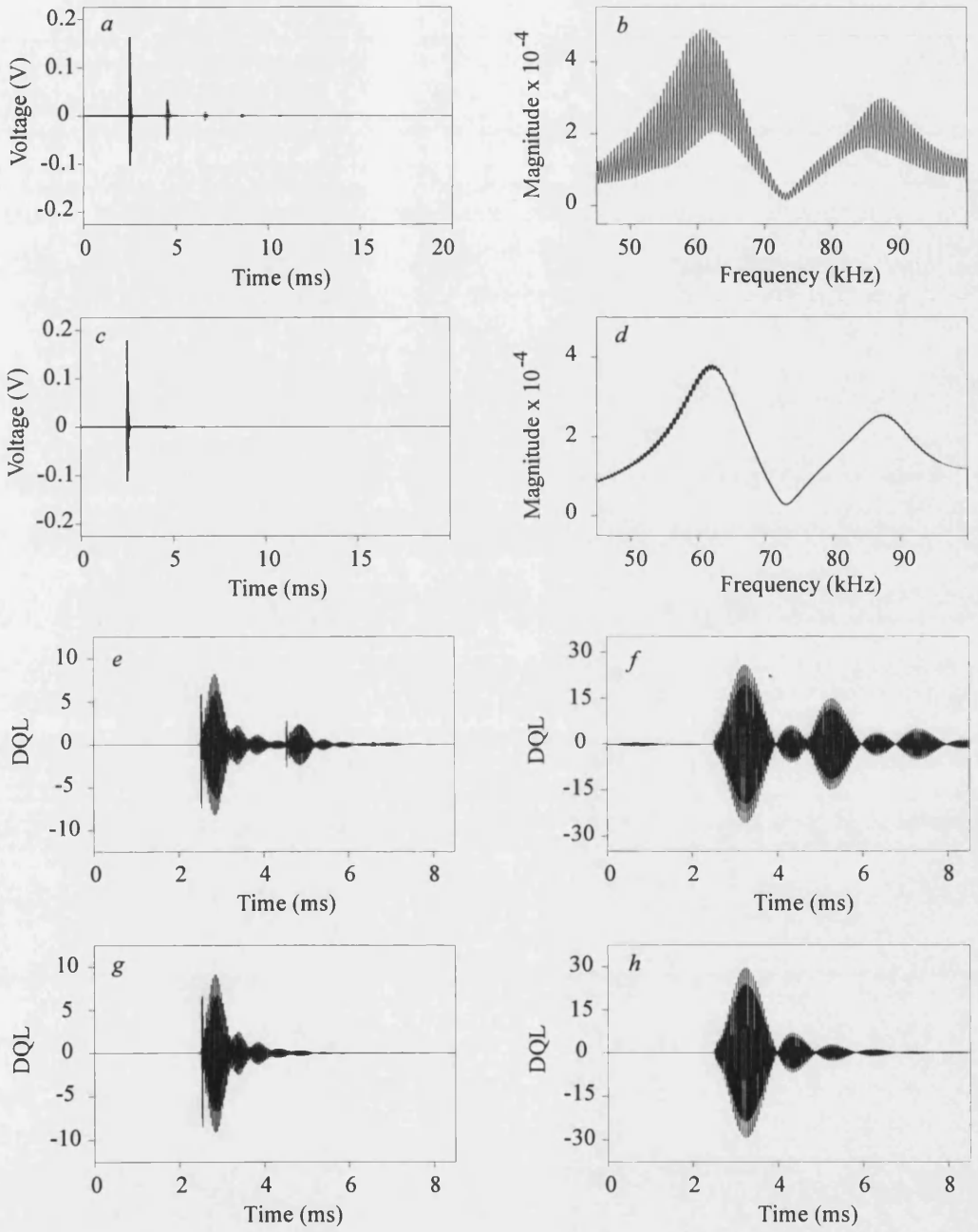
c End S a-phase capacitor voltage

d End S a-phase capacitor current

e End S MOV / bypass current

Fault inception, T_f = 2.5 ms

Figure 6.4 Typical external faulted phase voltage and current



a Mode 2 analogue signal

b Frequency spectrum of *a*

c Mode 3 analogue signal

d Frequency spectrum of *c*

e Mode 2 operate filter ouput

f Mode 2 restraint filter output

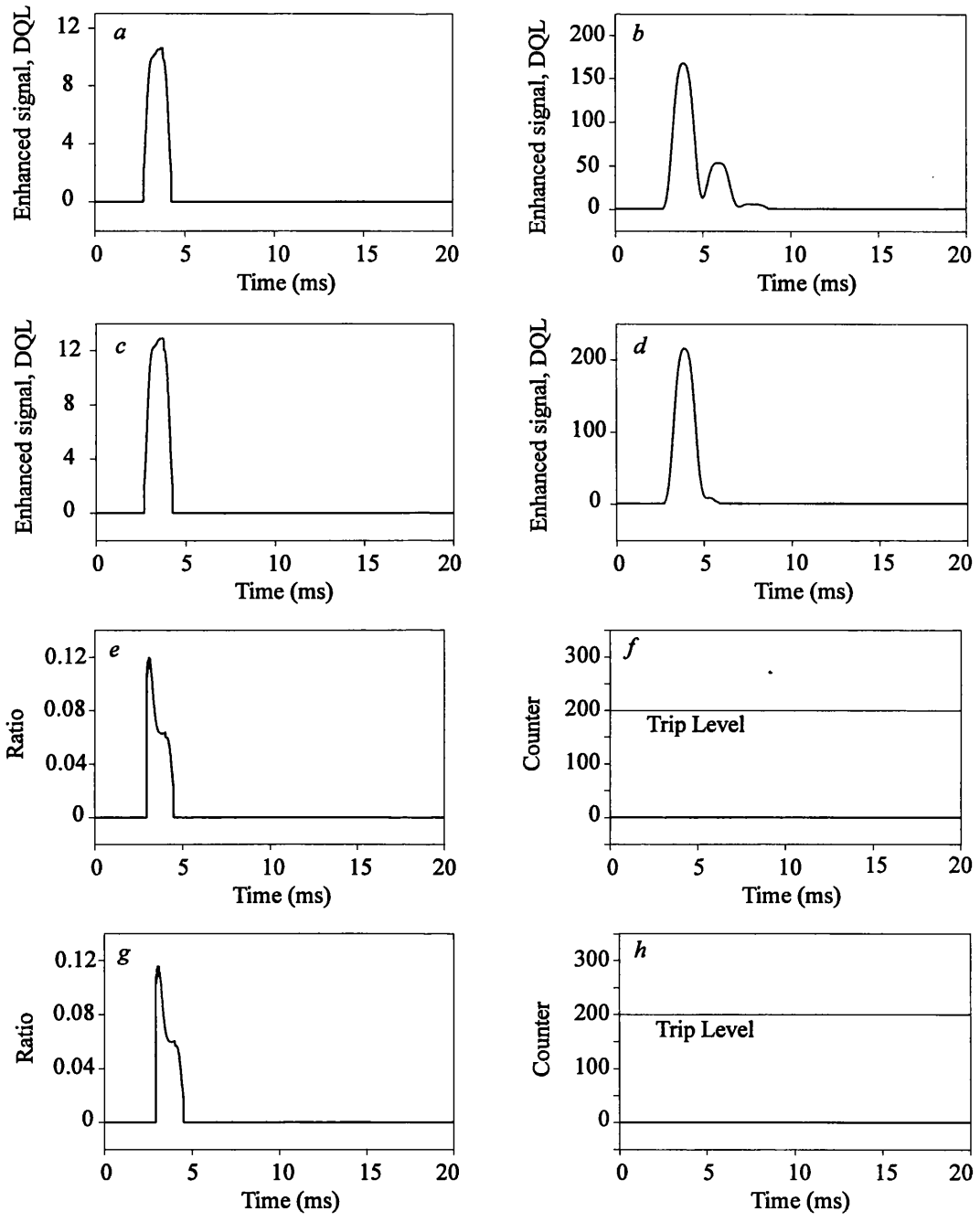
g Mode 3 operate filter output

h Mode 3 restraint filter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 6.5 Typical external fault response



a Mode 2 enhanced operate filter output *b* Mode 2 enhanced restraint filter output

c Mode 3 enhanced operate filter output *d* Mode 3 enhanced restraint filter output

e Mode 2 discrimination ratio *f* Mode 2 trip counter output

g Mode 3 discrimination ratio *h* Mode 3 trip counter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

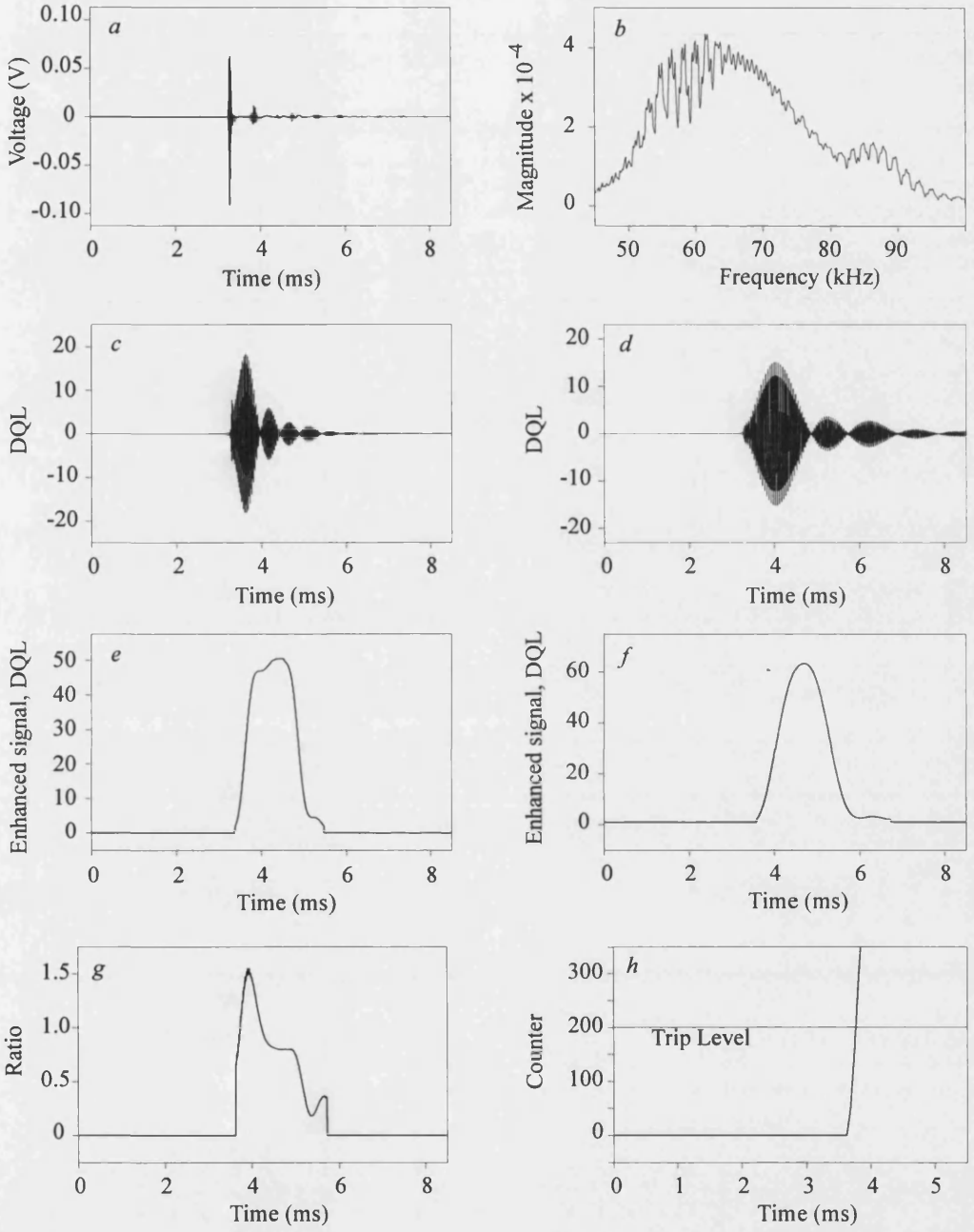
Figure 6.6 Typical external fault response

6.4 The Effect of Fault Inception Angle

The magnitudes of travelling waves generated on a transmission line are very much dependent on point on wave fault inception angles. In principal, faults occurring near voltage maximum give rise to the largest travelling waves and those near voltage zero to the minimum. Therefore, the performance of protection relays based on travelling waves suffers for faults near voltage zero owing to the sensitivity limitations imposed by the latter. However, the relay described here is highly dependent on measuring from bursts of HF fault generated signals created by nonlinear arcing faults (over 90% of faults are arcing faults). Such bursts of energy are, to a large extent, independent of the fault inception angle. This section examines a number of different faults to demonstrate the effect of fault inception angle on the relay performance.

6.4.1 Internal Fault

In section 6.2, an internal 'a'-phase to earth fault near voltage zero (at F_1 in Figure 4.2a) has already been examined in some detail. This showed that the HF voltage signals generated were of relatively small magnitudes and there was a large dc offset on the faulted phase current (Figure 6.1b). The performance of relay at End S was shown for both the aerial modes in Figures 6.2 and 6.3. The corresponding relay performance at End R for this particular fault condition is shown in Figures 6.7 and 6.8. Comparing the intermediate signals with those at end S shows that there are small differences between the two ends.



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

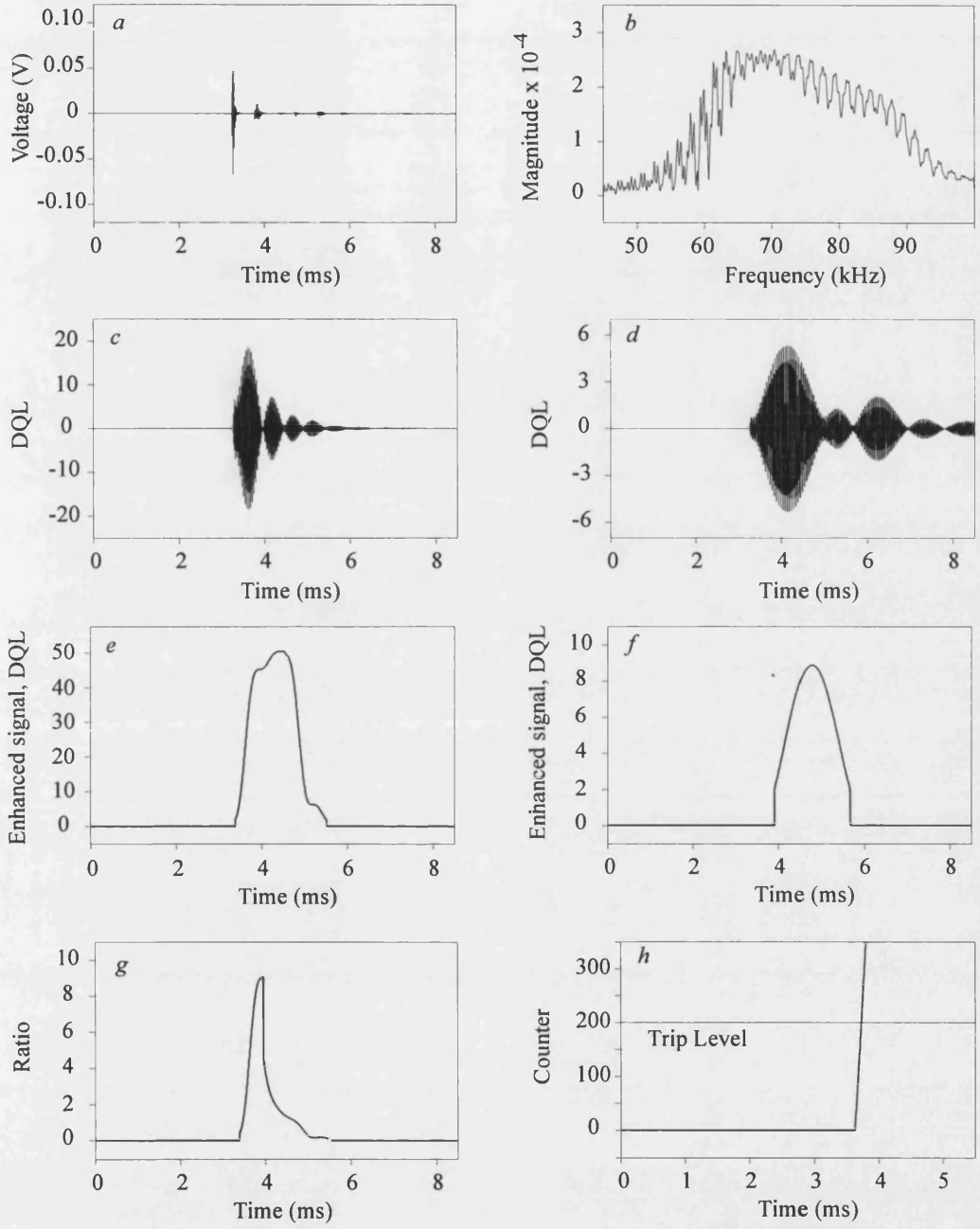
g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 6.7 Mode 2 relay response at end R for an internal fault near voltage zero



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

g Discrimination ratio

h Trip counter output

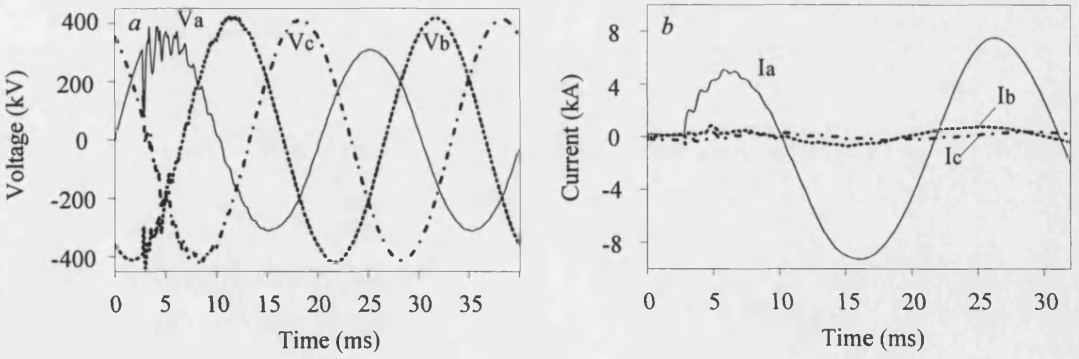
Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 6.8 Mode 3 relay response at end R for an internal fault near voltage zero

As evident from Figures 6.7a and 6.8a, the reduction in the signal magnitudes at End R has been caused by the attenuation of the longer line between fault point and end R. Moreover, it takes longer for the signals to arrive at end R than at end S because of the longer propagation delay time in the case of the former. The different reflections can also be seen and are further emphasised by the digital filter envelopes (Figures 6.7c,d, 6.8c,d). When the levels of the operate and restraint signals are observed, although the strengths of the signals have been reduced, their relative magnitudes remain approximately constant as evident from Figures 6.7e,f and 6.8e,f. Thus, there is little change to the discrimination ratios (Figures 6.7g, 6.8g) and the relay issues the trip decision in approximately 1 ms after fault inception.

Increasing the fault inception angle to 45^0 whilst keeping all the other parameters constant, has a significant effect on the signals generated. Considering the primary system voltage waveforms at end S, Figure 6.9 shows a significant HF distortion, and a lower dc offset on the current waveform.



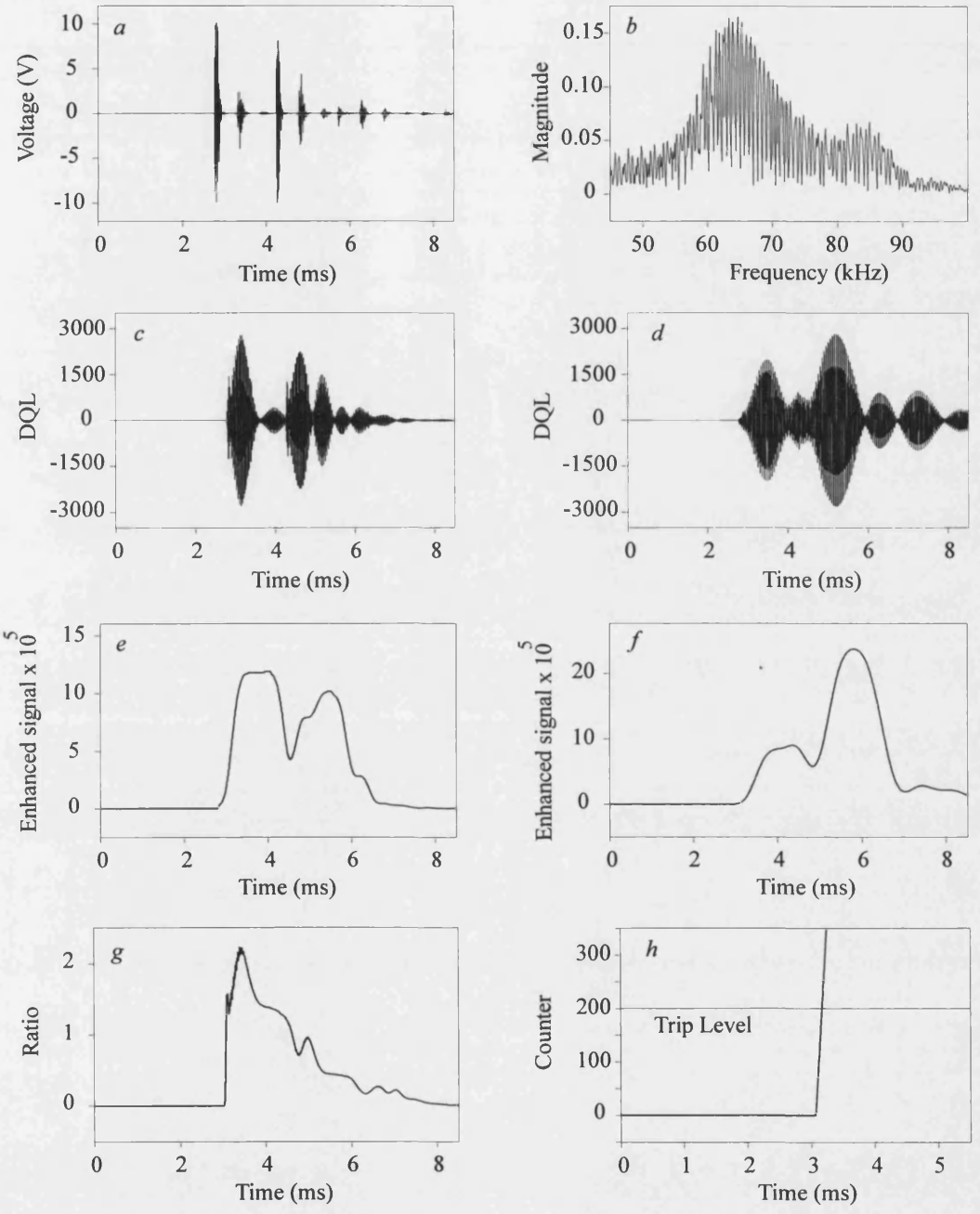
a End S phase voltages *b* End S phase currents

Fault inception, T_f = 2.5 ms

Figure 6.9 Phase voltage and current waveforms for an internal fault at 45^0

Figure 6.10 shows the relay performance associated with aerial mode 2 (V_x) signal at end S. The bursts of HF signals this time have a considerably larger magnitude and this is as a direct consequence of the signals being augmented by the presence of a significant travelling wave component. The successive bursts are also due to a combination of HF components generated by the non-linear behaviour of the primary arc and travelling wave components. These arise due to reflections from the impedance discontinuities in the circuit such as at the fault point and the line ends. The stack tuner output has been clipped to ± 10 V by the signal limiter and this manifests into some additional distortion which can be seen in the frequency domain (Figures 6.10a, b). The filter outputs are approximately two orders of magnitude larger than those for the near voltage zero fault case (Figures 6.10c, d) and the enhanced filter outputs are up to five orders of magnitude larger (Figures 6.10e, f). The discrimination ratio is well above unity and the trip decision is again given in approximately 0.6 ms after fault inception.

At end R, the signals have similar magnitudes to those at end S, although they are further delayed by the additional travel time (Figures 6.11). The additional line attenuation also means that less clipping is required, reducing the amount of distortion (Figures 6.11a, b). The filter outputs are, therefore, marginally lower and the discrimination ratio peaks at approximately 1.2; a trip decision is given in approximately 1 ms after fault inception (Figures 6.11g, h).



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

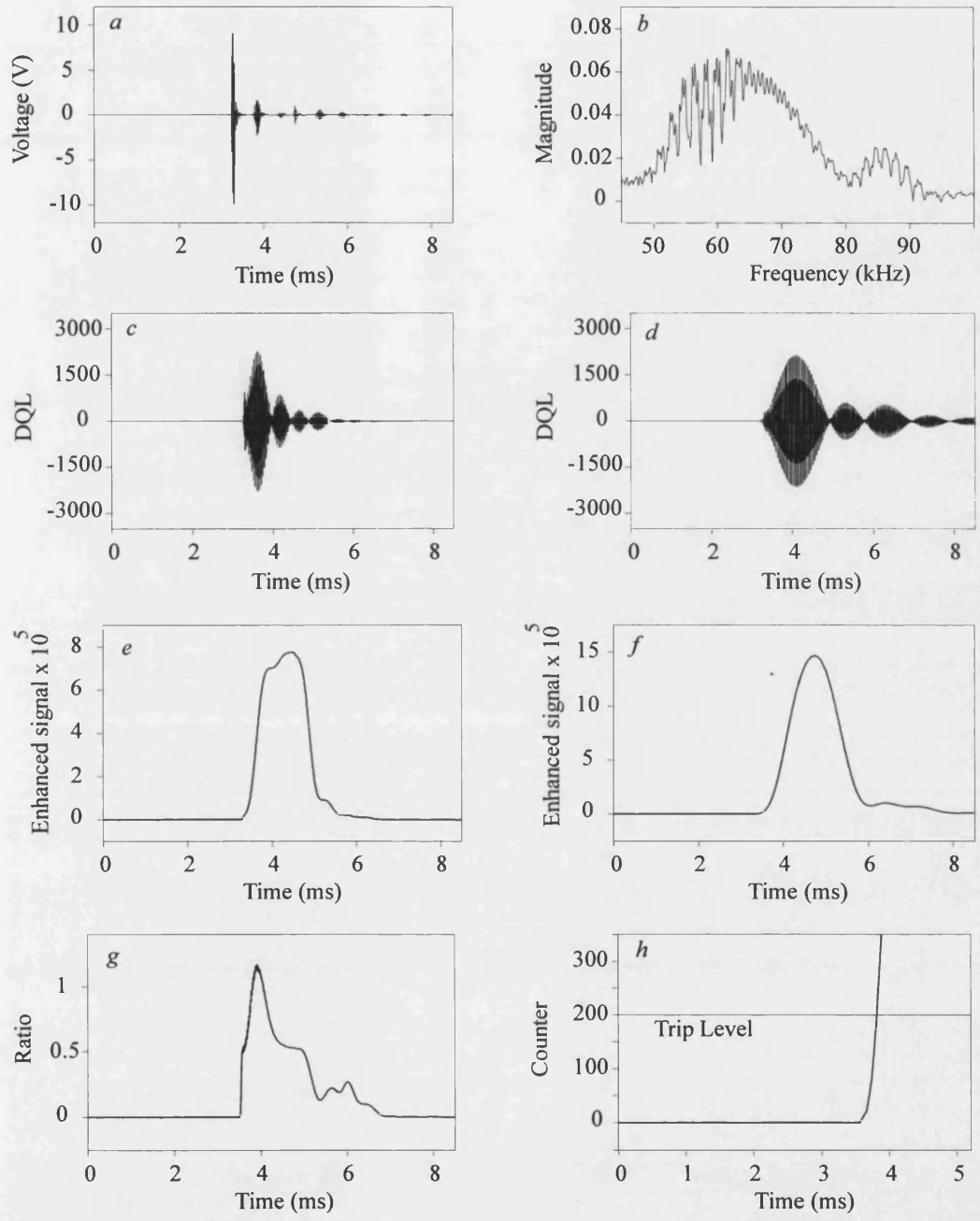
g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 6.10 Mode 2 relay response at end S for an internal fault at 45^0



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

g Discrimination ratio

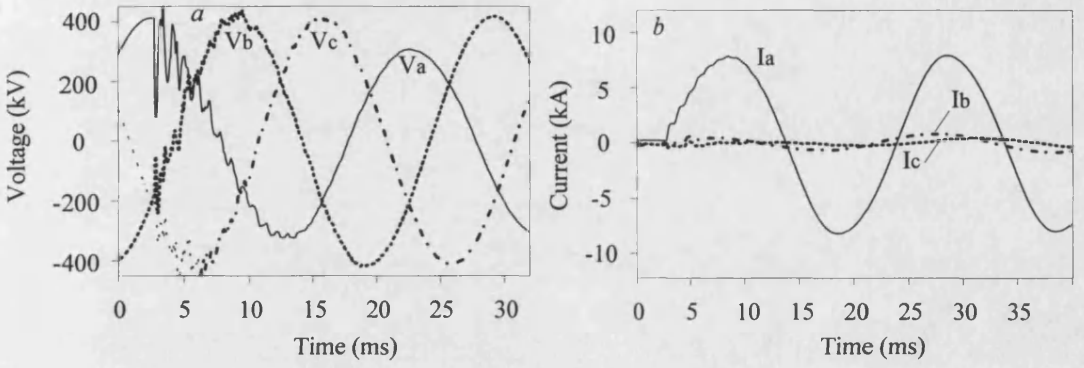
h Trip counter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 6.11 Mode 2 relay response at end R for an internal fault at 45^0

Figure 6.12 shows the primary system voltage for the same fault occurring near voltage maximum (ie. inception angle is 90^0). In this case, the amount of voltage transients increase further and there is virtually no dc offset on the current waveform as shown in Figure 6.12b.



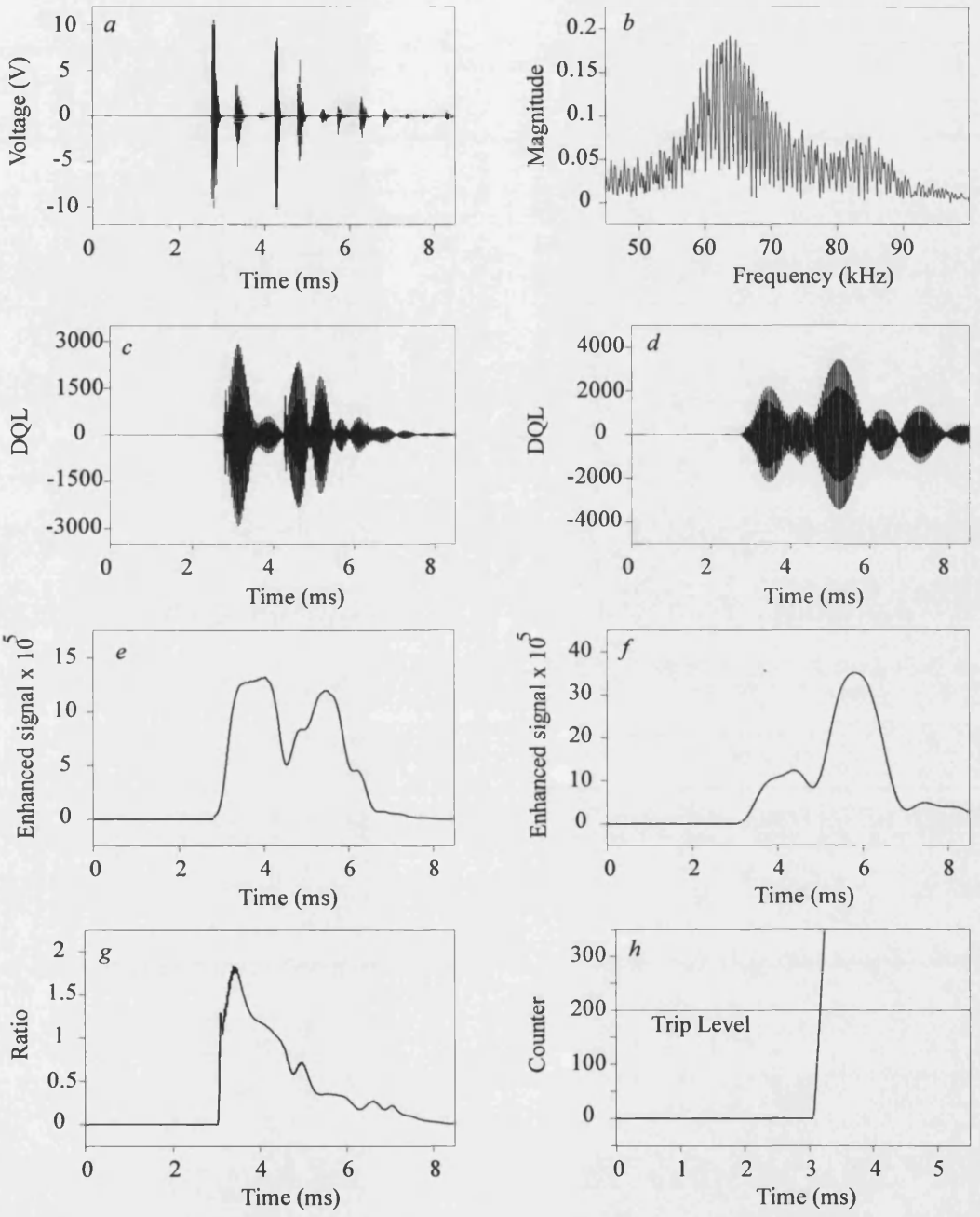
a End S phase voltages *b* End S phase currents

Fault inception, T_f = 2.5 ms

Figure 6.12 Phase voltage and current waveforms for an internal fault near voltage maximum

Therefore, the HF noise captured by the stack tuner this time have a much larger magnitude but they are limited to ±10 V during the quantisation process (Figure 6.13a). The increase in the signal magnitudes associated with the larger fault inception angle are therefore minimised. The basic nature of the signals however remains the same and a discrimination ratio of approximately 1.8 is achieved giving a trip decision in approximately 0.6 ms after fault inception.

The waveforms are again somewhat similar at end R for the same fault case (Figure 6.14) and as expected, the additional attenuation and delays as for the other fault inception angles are again present.



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

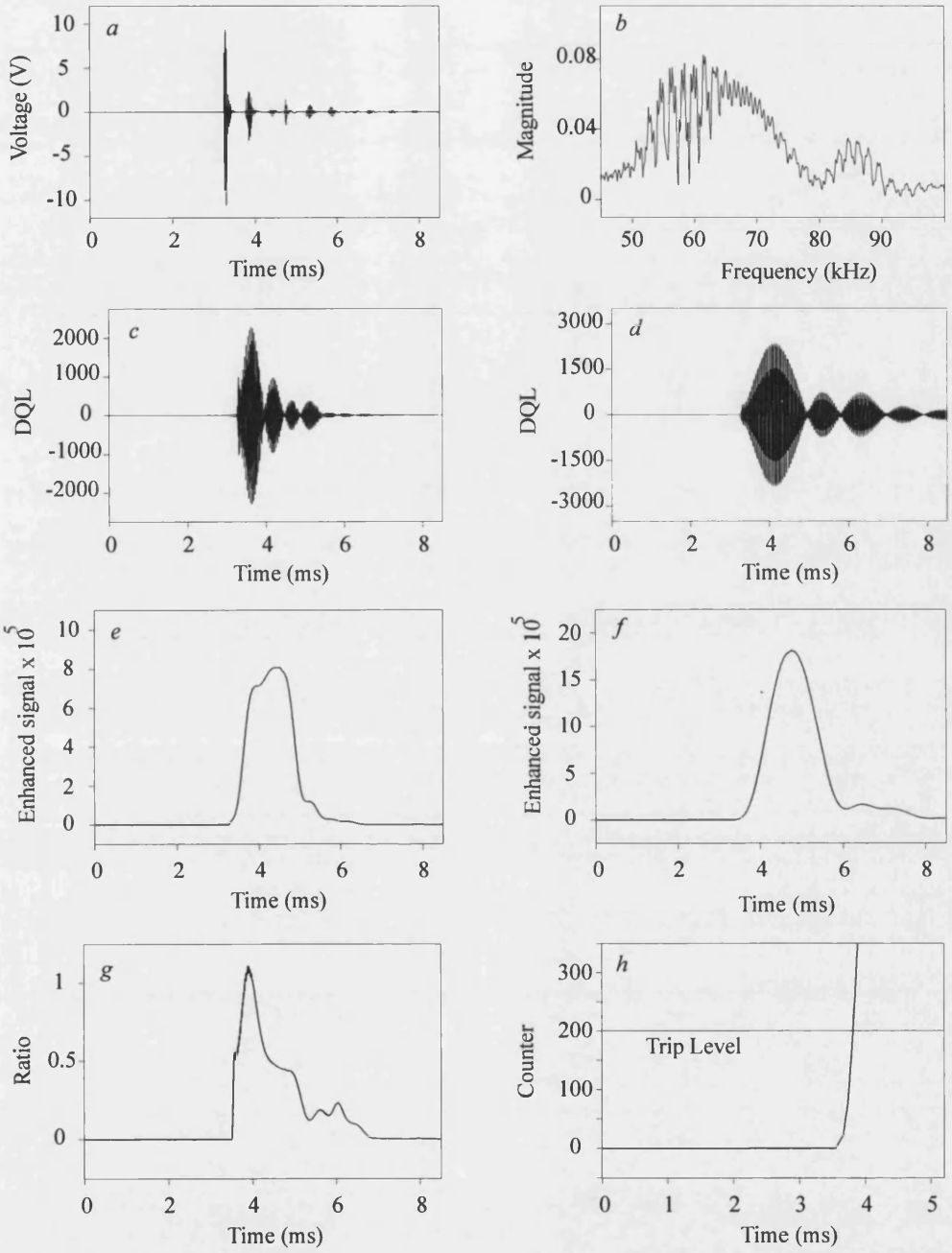
g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 6.13 Mode 2 relay response at end S for an internal fault near voltage maximum



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

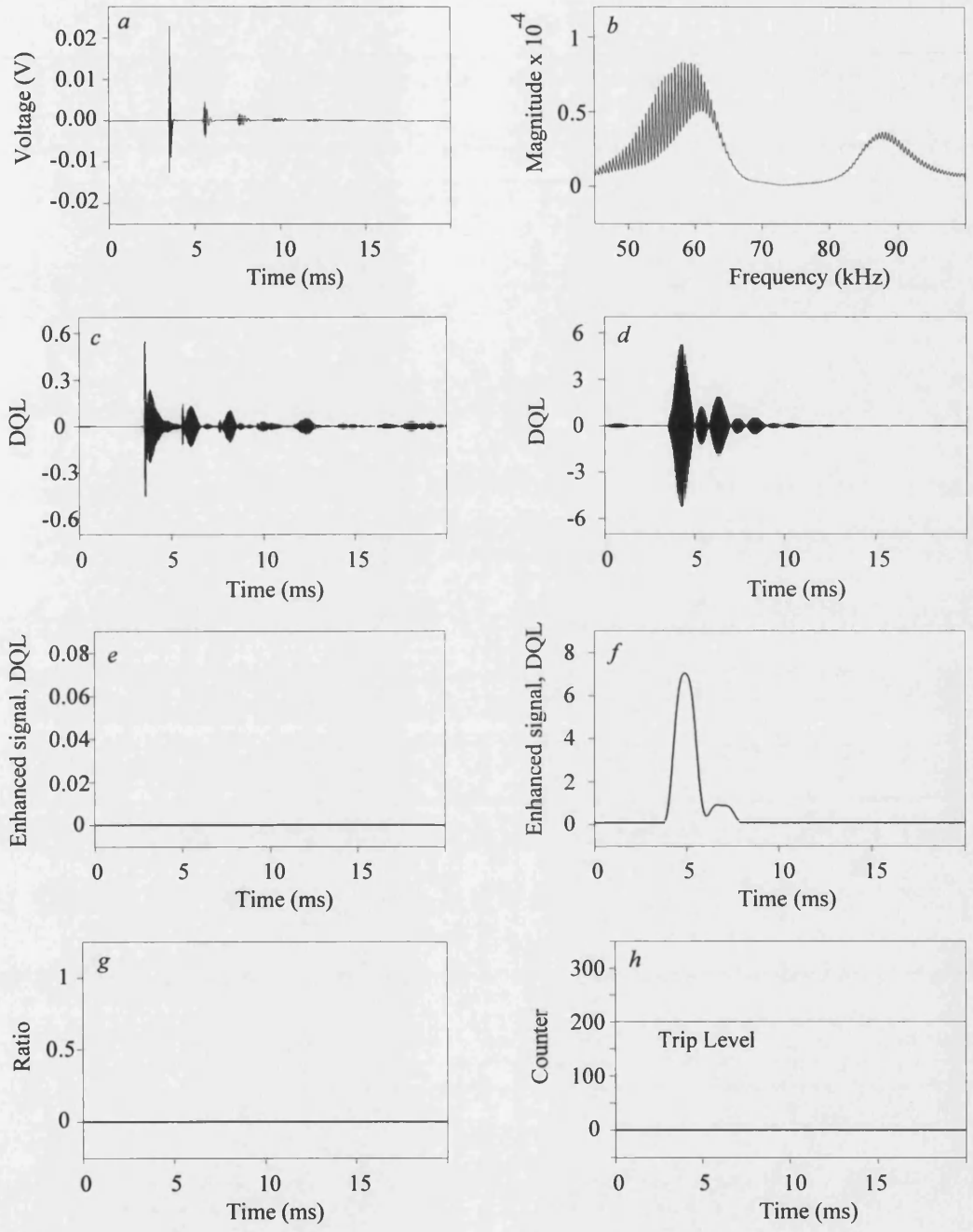
DQL = Digital quantum levels

Figure 6.14 Mode 2 relay response at end R for an internal fault near voltage maximum

6.4.2 External Fault

An external 'a'-phase to earth fault near voltage zero at F_2 in Figure 4.2a has been discussed in some depth in section 6.3. The fault was applied just behind the line trap at end S external to the protected zone and the two aerial mode signals V_x and V_y at end S have already been examined. The relay response at end R for the same fault is shown in Figures 6.15 and 6.16 for both modes, respectively.

The waveforms are essentially the same as those at end S except that the magnitudes are reduced by the waves propagating through a longer line length with the associated increase in the transit time. As expected, in all the cases, there is severe attenuation of the narrow frequency band around 75 kHz for the external fault. The operate filter output associated with mode V_x is very low (Figure 6.15c), falling below the minimum threshold set within the relay algorithm; thus the enhanced operate filter output is forced to zero (Figure 6.15e). The discrimination ratio, therefore, stays at zero and no trip decision is issued (Figures 6.15g, h). However, operate filter output associated with mode V_y has a slightly higher value (just above the threshold) and there is thus a finite value for the enhanced operate filter output (Figures 6.16c, e). However, the latter is much less than that of restraint signal and therefore the discrimination ratio remains well below unity and so no trip decision is given (Figure 6.16g, h).



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

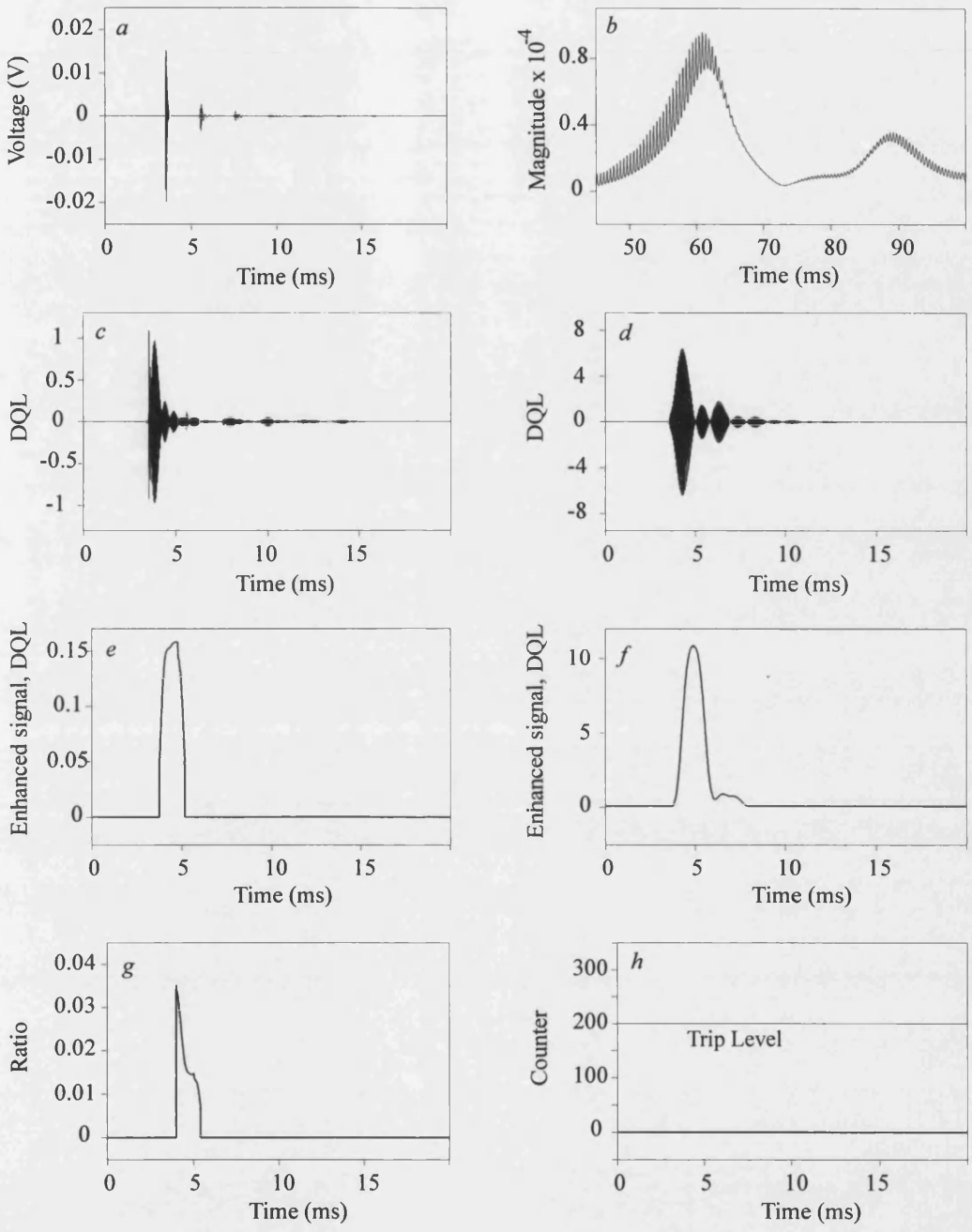
g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 6.15 Mode 2 relay response at end R for an external fault near voltage zero



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

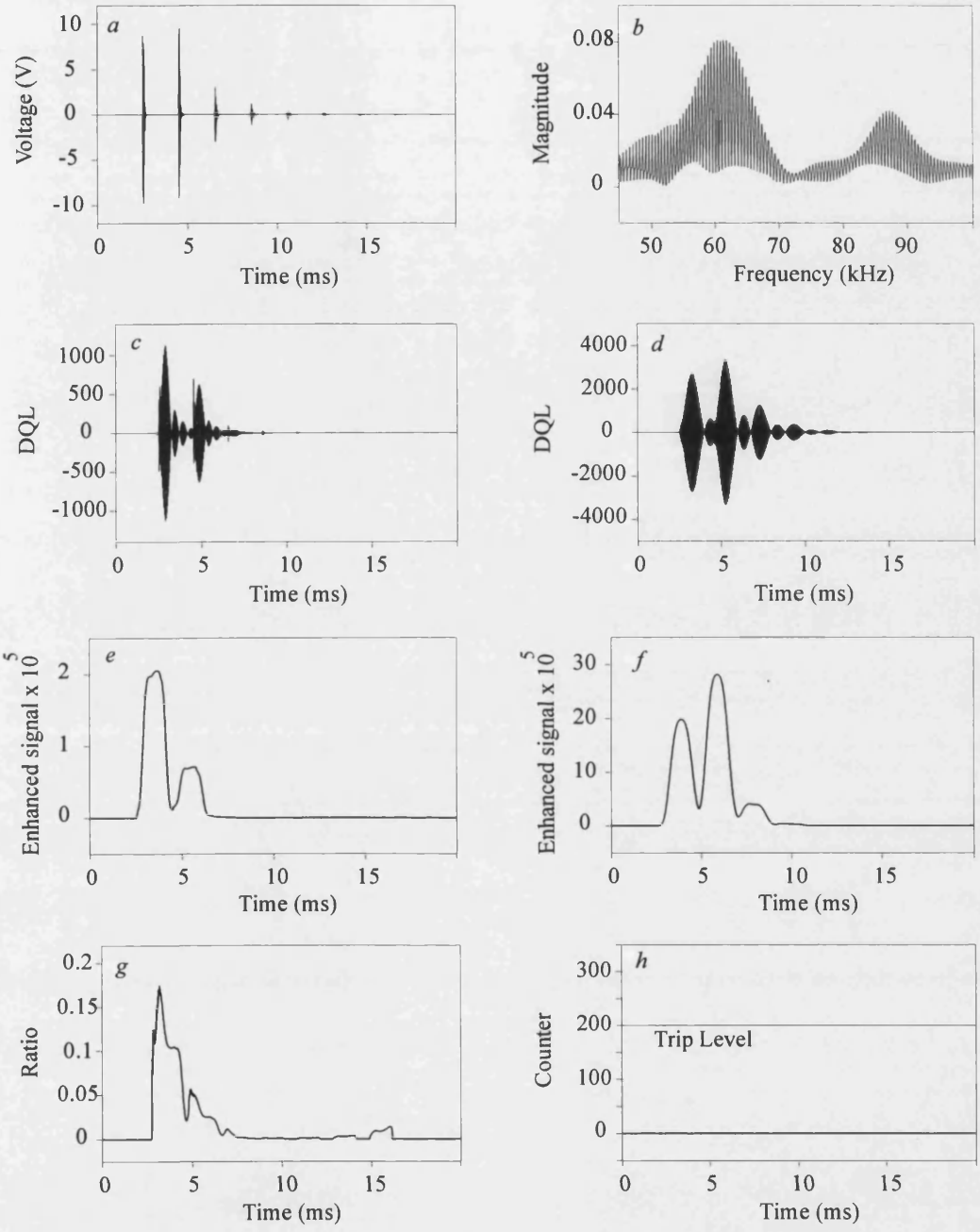
DQL = Digital quantum levels

Figure 6.16 Mode 3 relay response at end R for an external fault near voltage zero

When the fault inception angle is increased to 45^0, the mode V_x stack tuner output at end S is considerably increased as shown in Figure 6.17a. The signal has to be clipped to limit it to ± 10 V but this does not significantly distort its frequency domain profile (Figure 6.17b); more importantly, the ratio between the operate and restraint signals is approximately 1:20 (Figures 6.17e, f) ie. the discrimination ratio peaks at just below 0.2, and hence no trip decision is issued (Figures 6.17g, h).

Considering the mode 2 signal V_x at end R for the same fault case, the magnitudes of the HF bursts are again attenuated by the longer line length and they are less than ± 10 V (Figure 6.18a). Therefore, there is no clipping of the signals and this effectively means that there is no distortion in the frequency response (Figure 6.18b). In this case, the ratio of the restraint filter output to the operate filter output is approximately 400:1 (Figures 6.18e, f). The net effect is that the discrimination ratio stays very close to zero and as a consequence, the counter outputs remain at zero as shown by Figure 6.18g, h.

Increasing the fault inception angle to 90^0 does not have any significant bearing on the stability of the relay. Figures 6.19 and 6.20 show the mode 2 signals at end S and R respectively. As expected, although the signal levels are increased by the additionally generated HF components and trip counters at both ends S and R remain at zero.



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

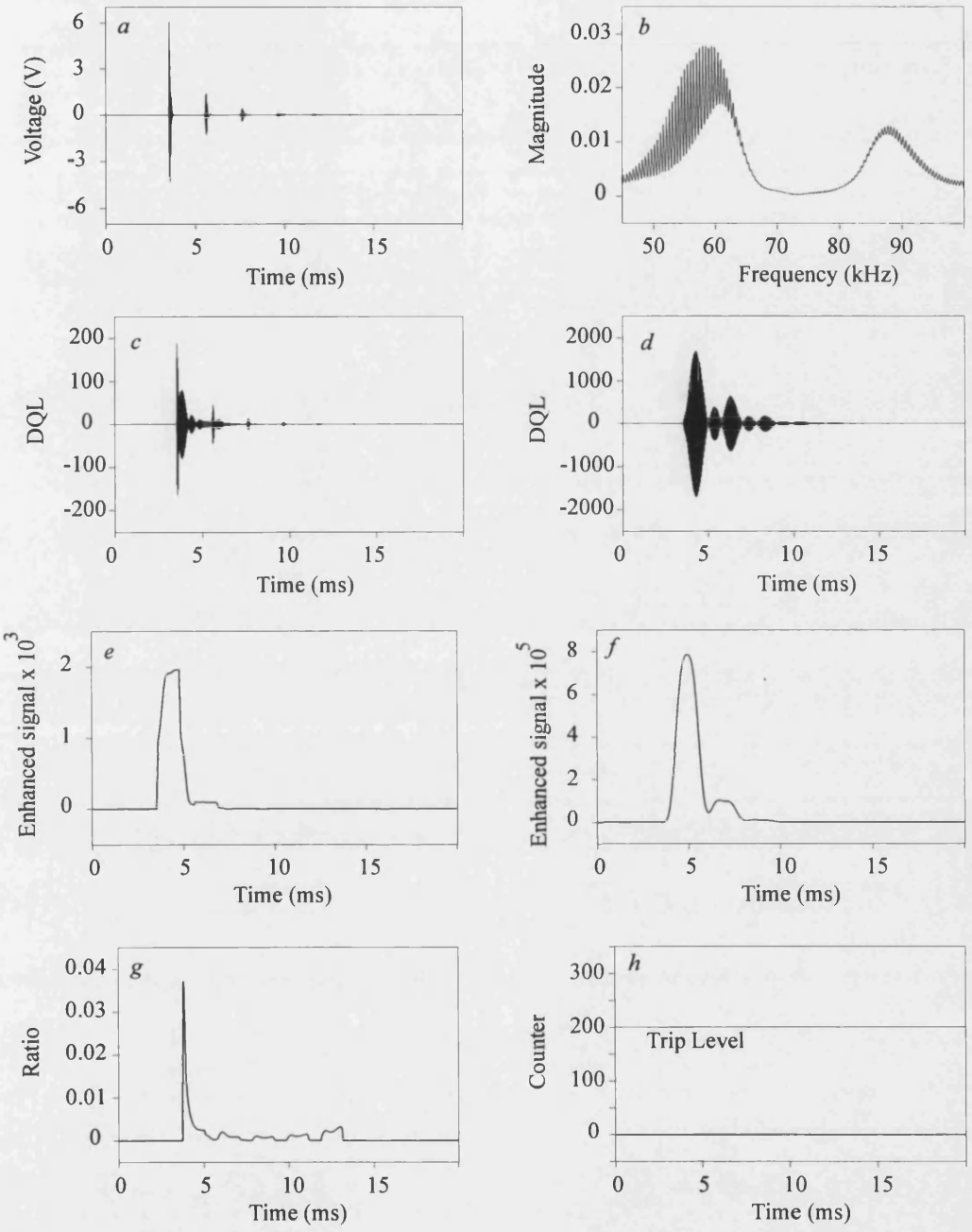
g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 6.17 Mode 2 relay response at end S for an external fault at 45^0



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

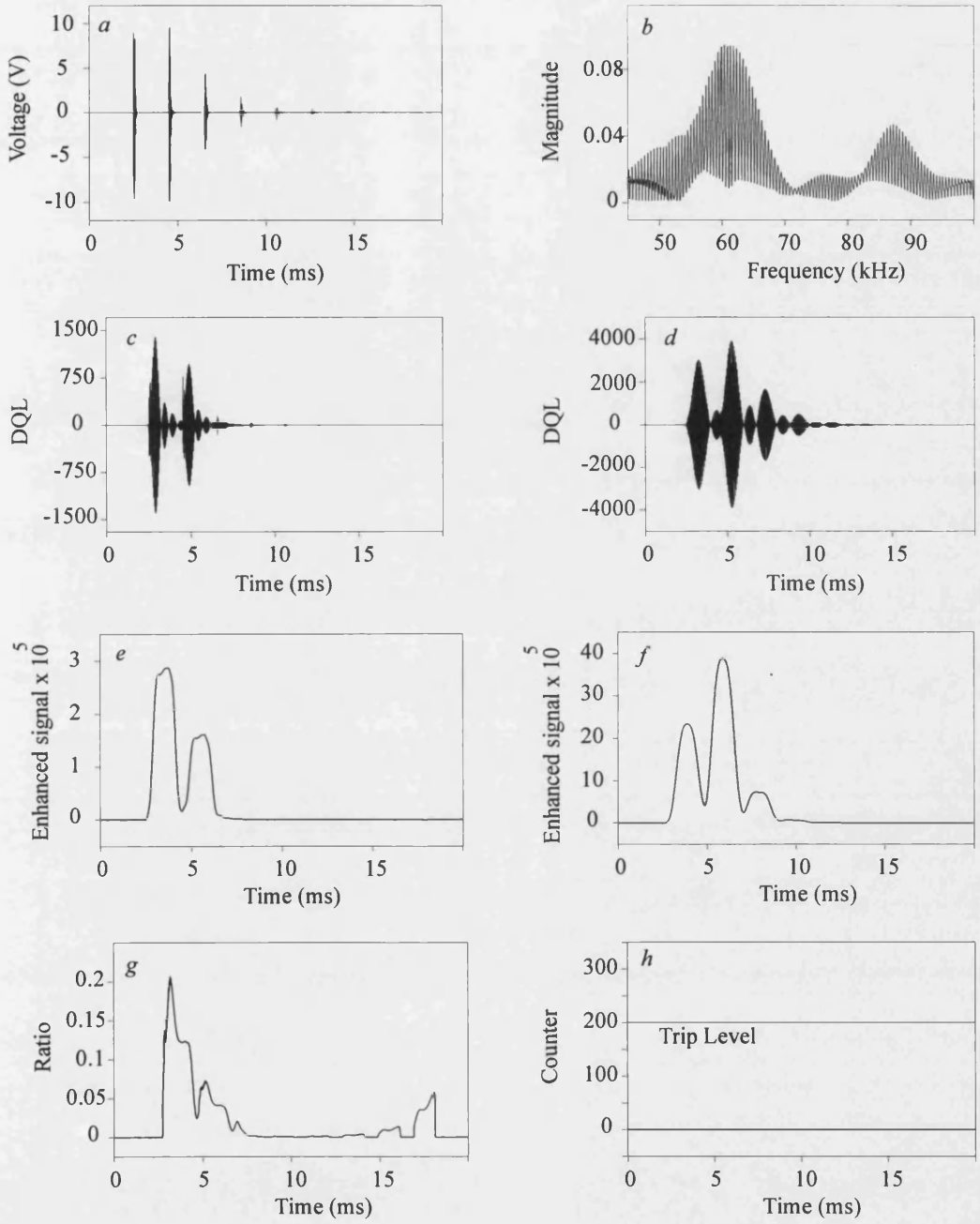
g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 6.18 Mode 2 relay response at end R for an external fault at 45^0



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

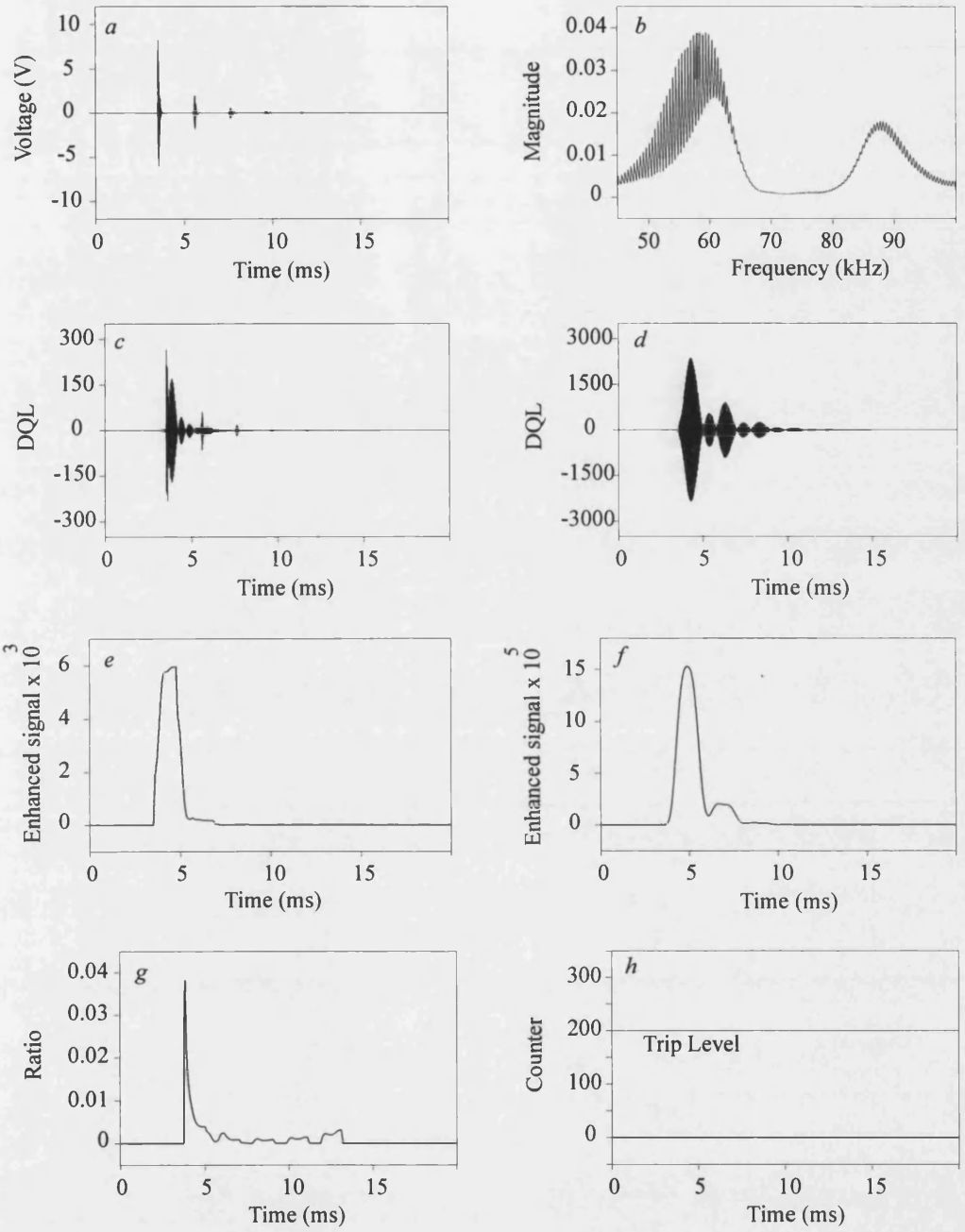
g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 6.19 Mode 2 relay response at end S for an external fault near voltage maximum



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

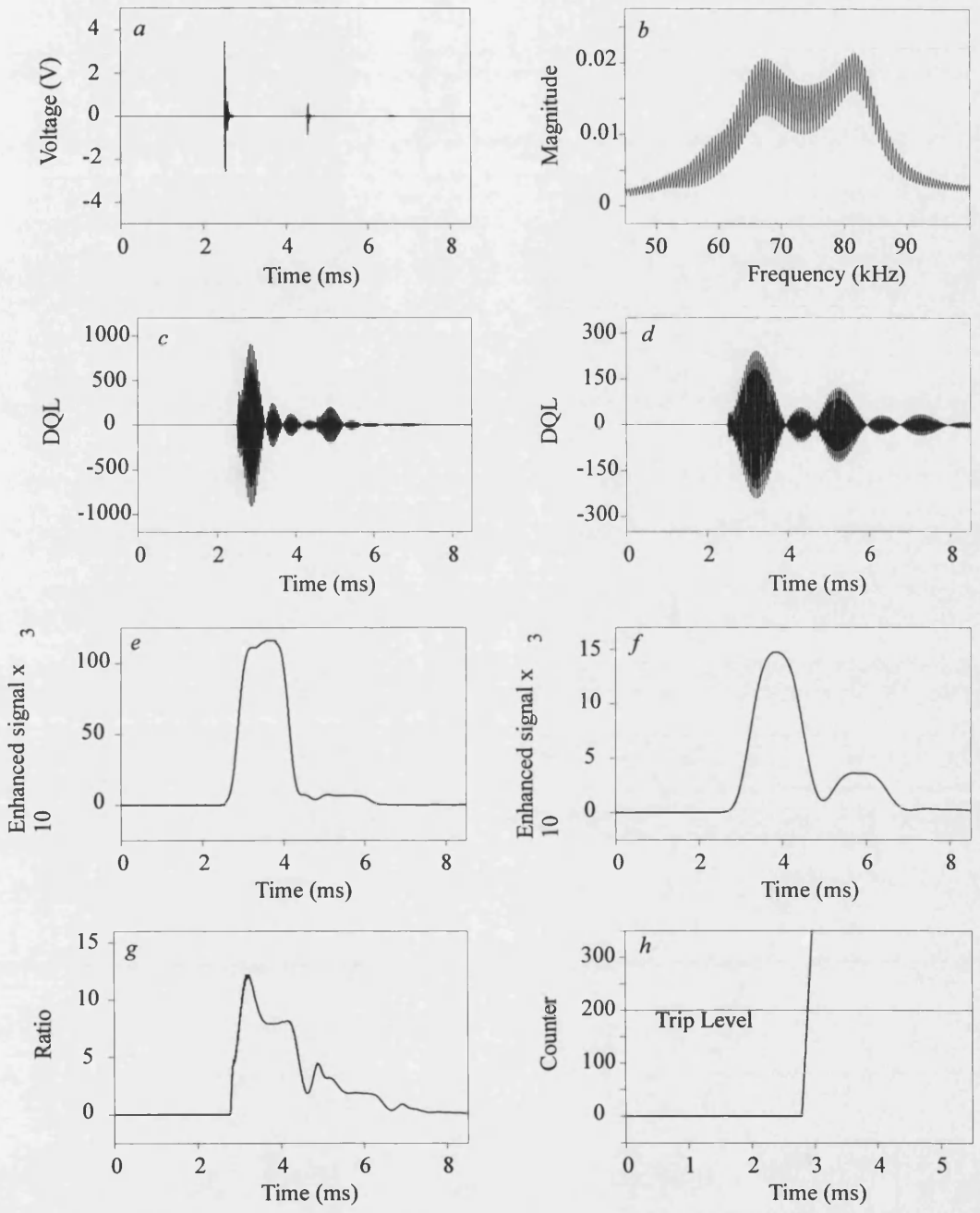
Figure 6.20 Mode 2 relay response at end R for an external fault near voltage maximum

6.5 The Effect of Fault Position

The position of the fault has a distinct effect on the nature of the signals detected by the stack tuners. As discussed previously, the most significant differences are observed between an internal and external fault to the protected zone. There are, however, small differences between the waveforms, for internal fault, depending upon the fault position. The differences in the captured signals can be examined by comparing all the mode 2 signal (V_x) at end S and R for internal faults at three different positions on the typical multi-section EHV feeder system shown in Figure 4.2b. They are all 'a'-phase to earth faults with a near zero fault inception angle and are applied: i, very close to sending end capacitor (at F_5), ii, 100 km from end S (at F_6) and iii, 180 km from end S (at F_7).

The waveforms at each stage within the relays at end S and R for a fault at F_5 are shown in Figures 6.21 and 6.22, respectively. Figures 6.23 and 6.24 show the corresponding relay results at two ends for the fault at F_6 while the results for a fault at F_7 are shown in Figures 6.25 and 6.26, respectively.

When these various faulted responses are examined, in keeping with the previous observations, it is apparent that as the distance from the relay measurement point to the fault point increases, the magnitudes of the HF signals decrease and their transit times increase. This is due to the attenuation factor associated with the line and the propagation velocities of the HF waves, respectively.



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

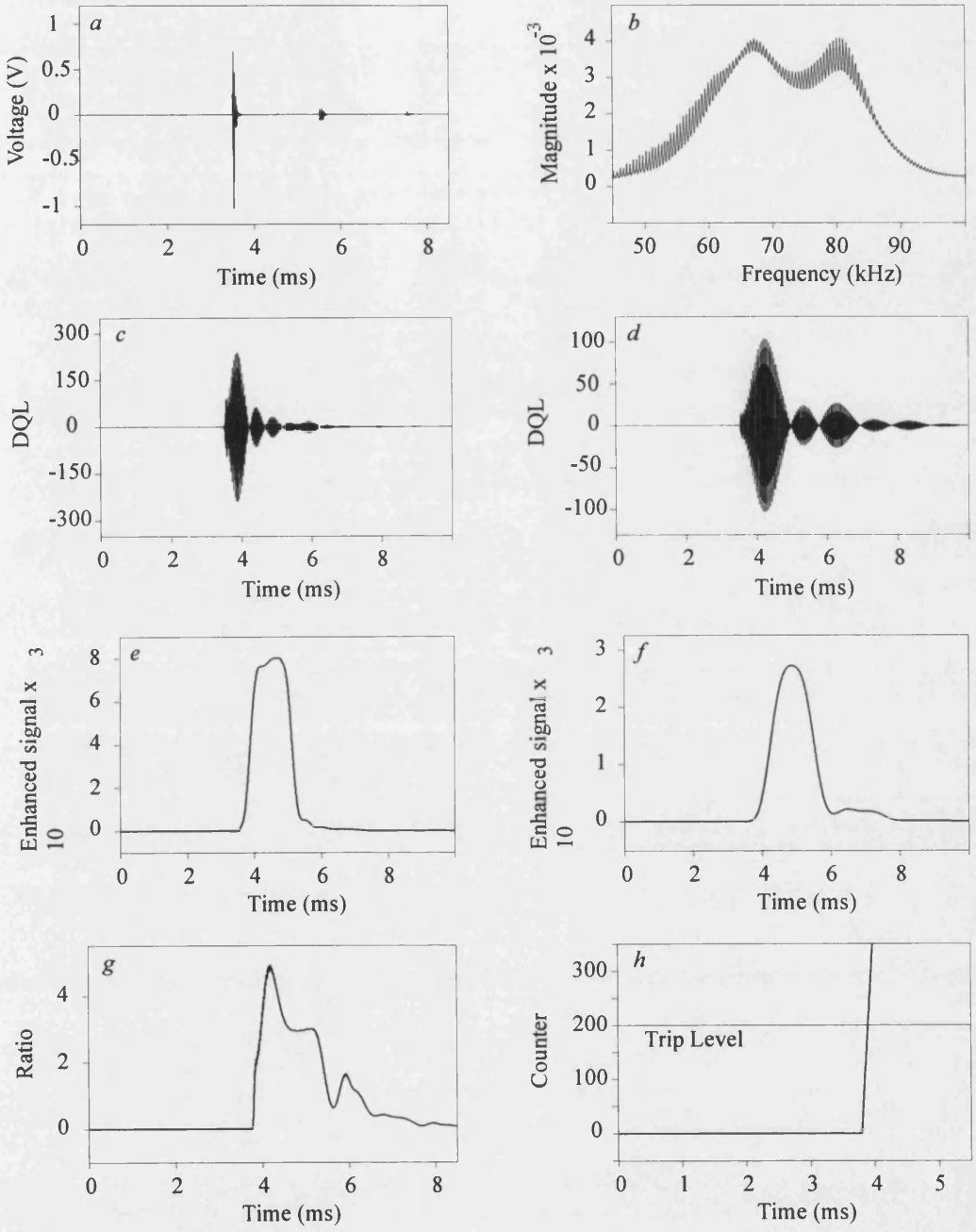
g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 6.21 Mode 2 relay response at end S for a fault at F_5



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

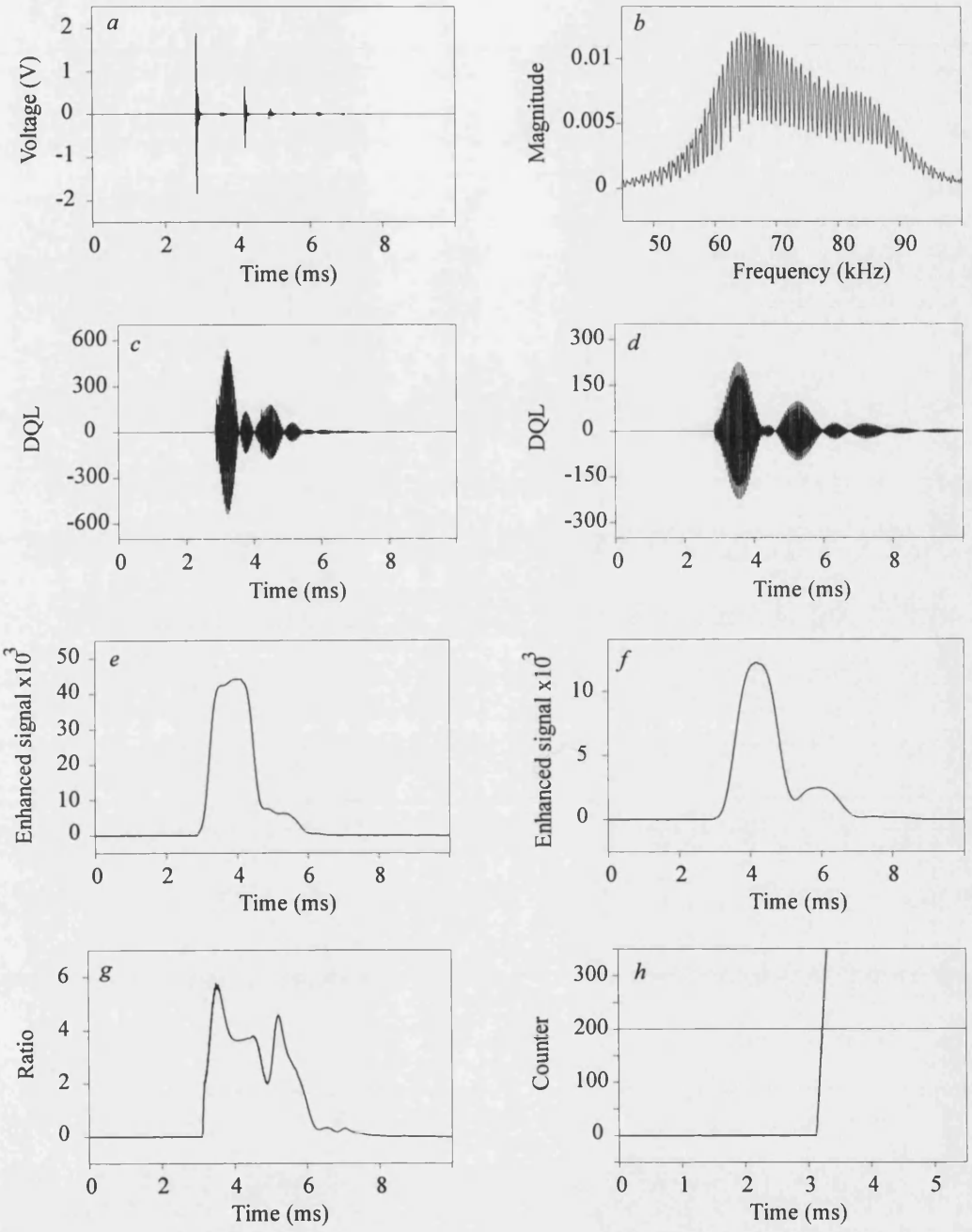
g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 6.22 Mode 2 relay response at end R for a fault at F_5



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

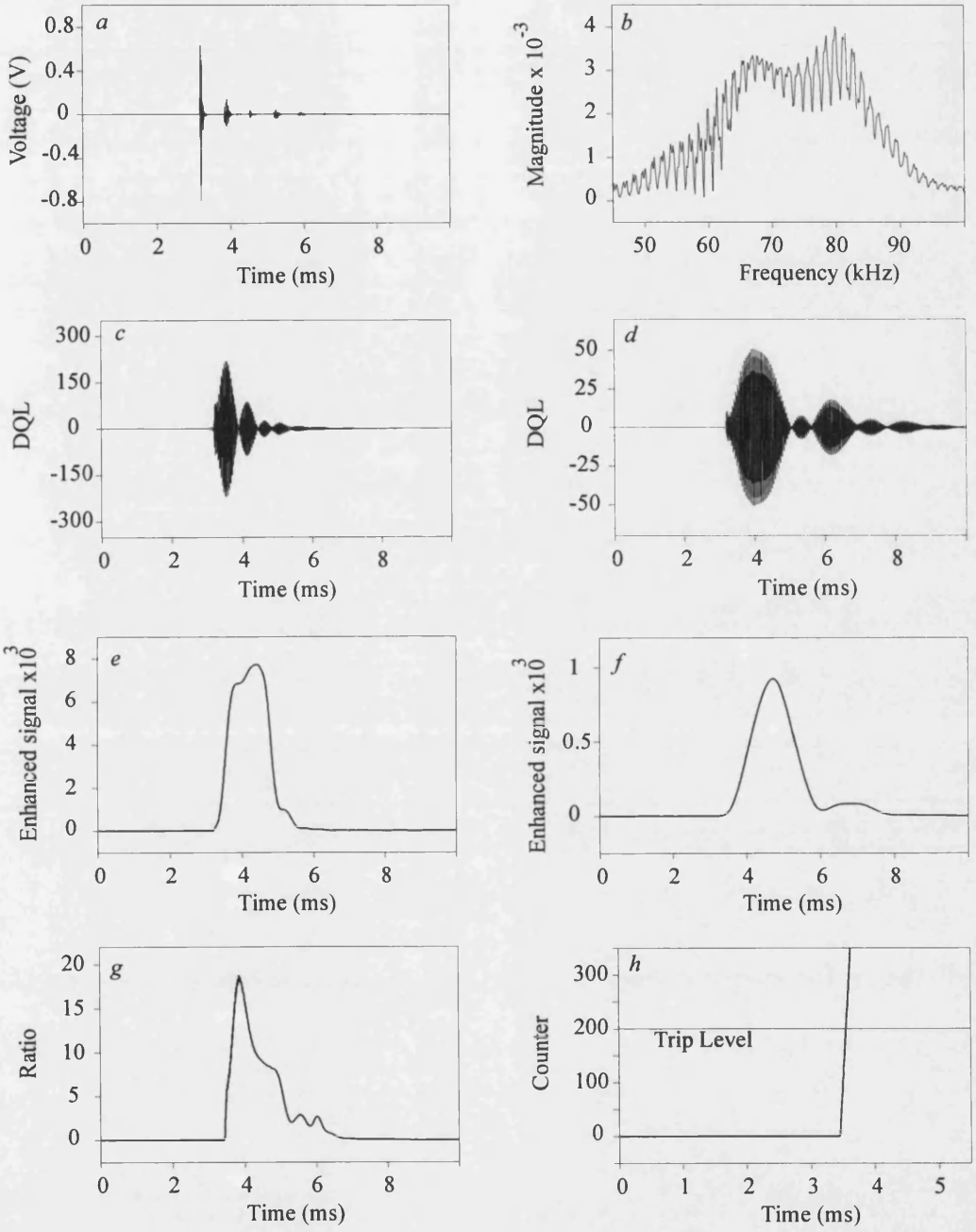
g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 6.23 Mode 2 relay response at end S for a fault at F_6



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

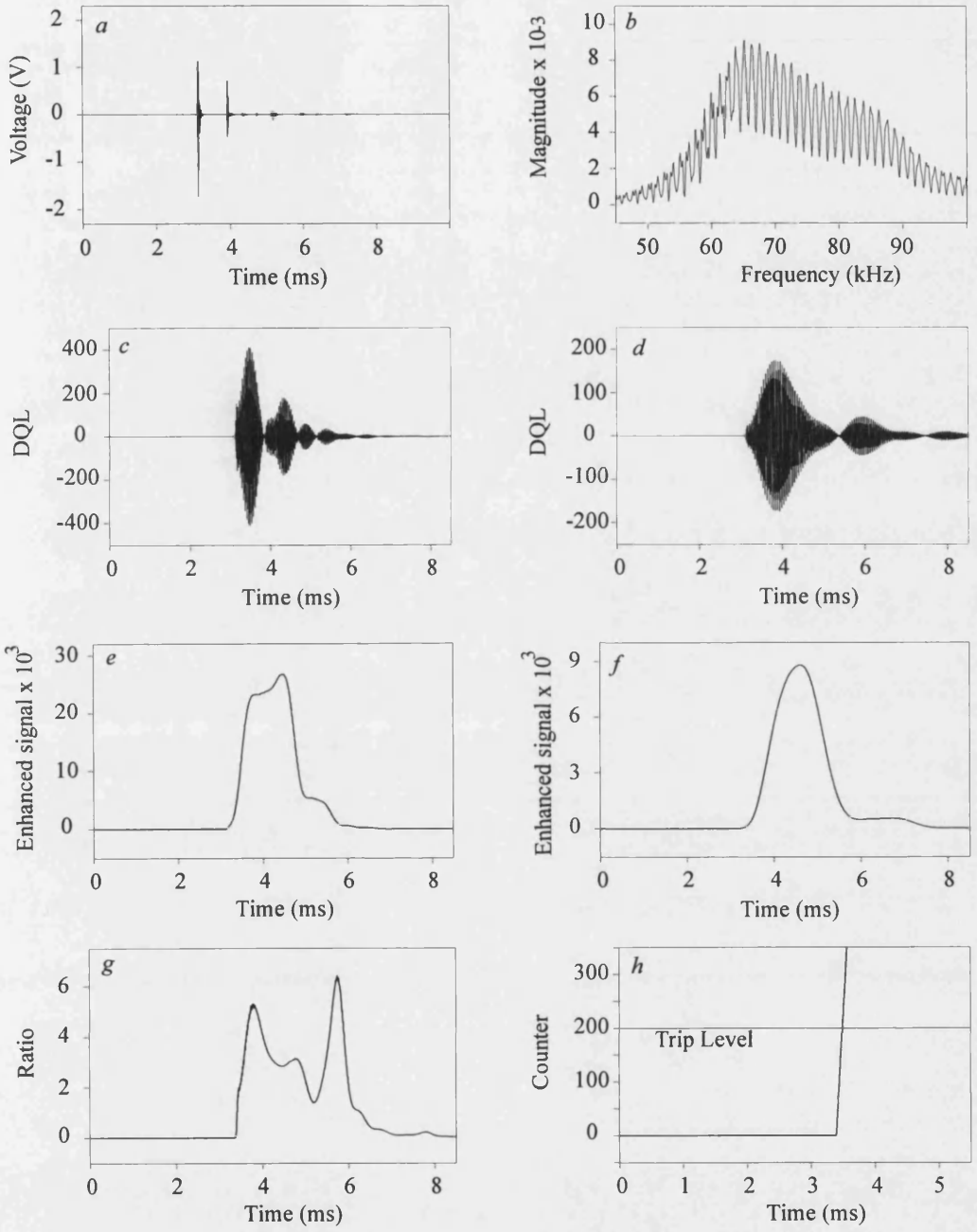
g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 6.24 Mode 2 relay response at end R for a fault at F_6



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

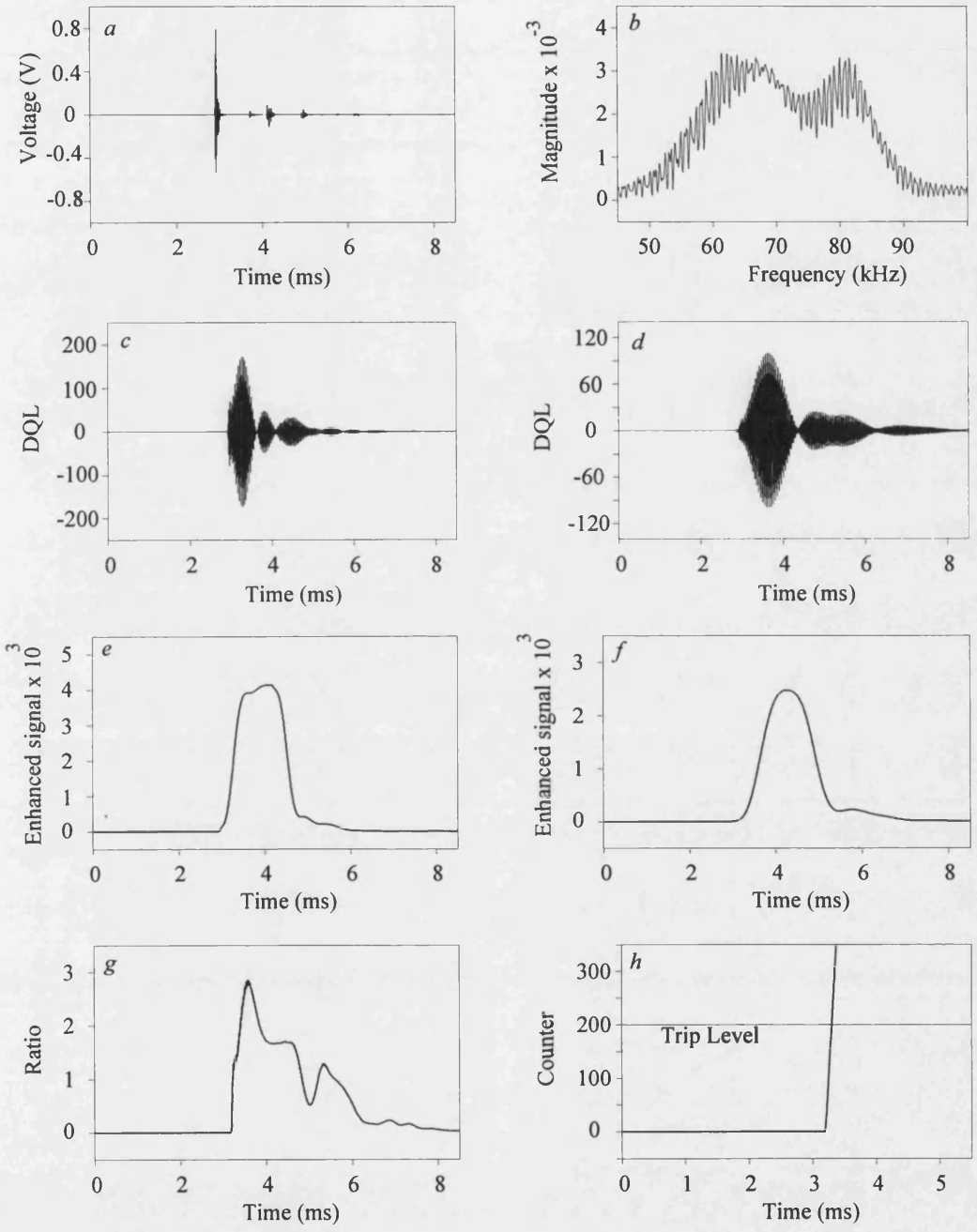
g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 6.25 Mode 2 relay response at end S for a fault F_7



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

g Discrimination ratio

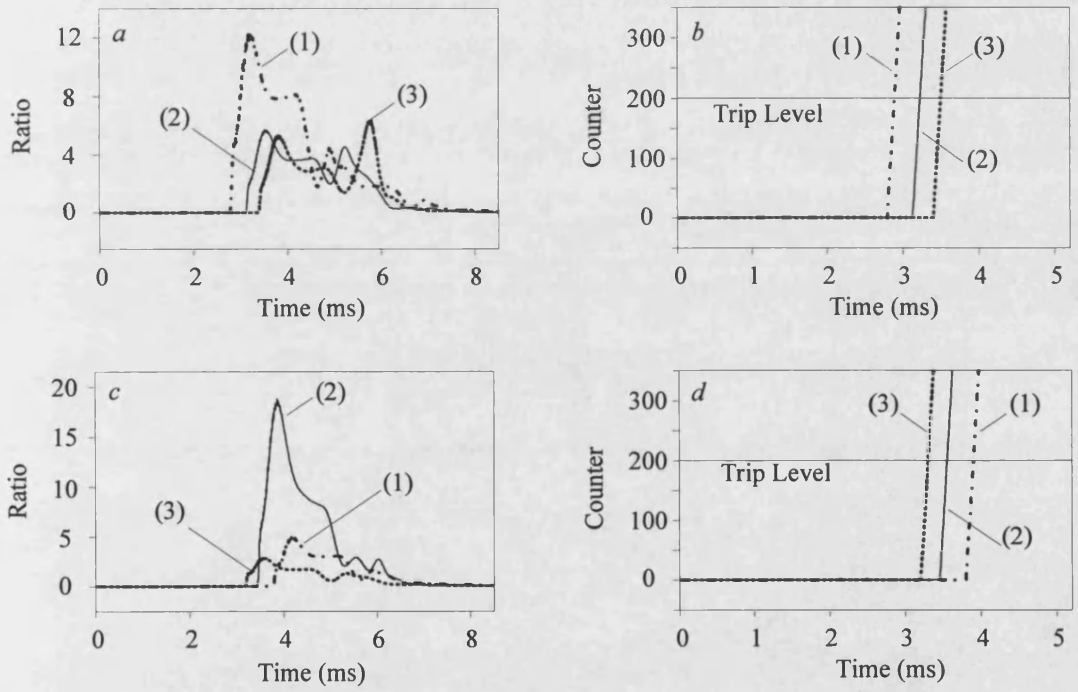
h Trip counter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 6.26 Mode 2 relay response at end R for a fault at F_7

Figure 6.27 shows a comparison of the discrimination ratios for these three faults, at end S and R with their corresponding trip counter outputs. As would be expected, the discrimination ratios are well above unity in all the cases and the trip decisions are asserted a short time after the occurrence of a fault. The variations in the discrimination ratios arise as a direct consequence of the small variations in the frequencies of the HF transients; the small variations in the trip times are by virtue of the variations in the transit times of the bursts of HF signals.



a End S discrimination ratios *b* End S trip counter outputs (1) Fault at F_5

c End R discrimination ratios *d* End R trip counter outputs (2) Fault at F_6

Fault inception, T_f = 2.5 ms (3) Fault at F_7

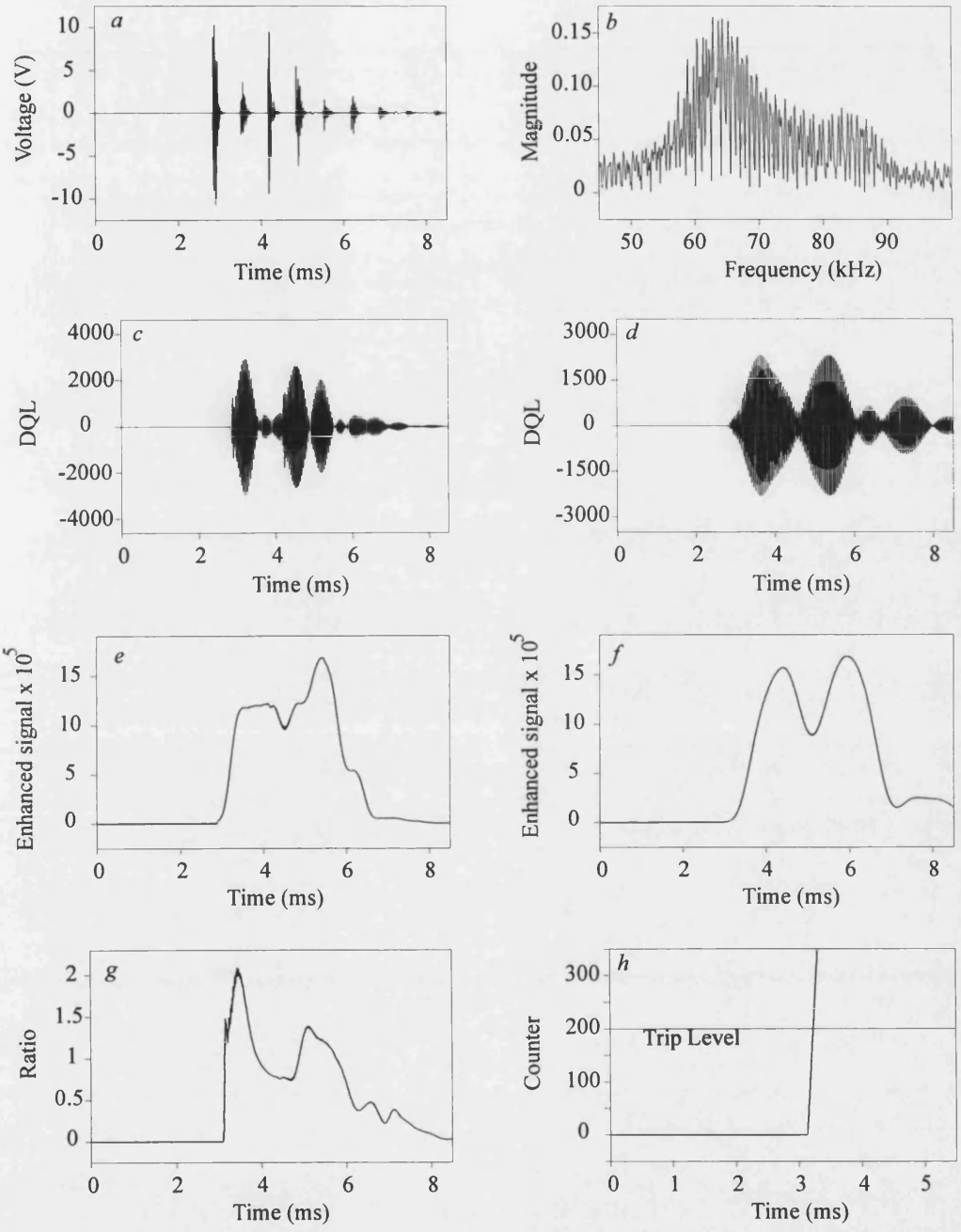
Figure 6.27 Effect of fault position on relay performance

6.6 The Effect of Fault Type

In practice, although most faults are of the single phase to earth type, other types of fault do occur and it is therefore important to examine the relay performance for other faults. In this section, the different types of fault are applied 60 km (at F_6) from end S on the multi-section system shown in Figure 4.2b; this is to examine the effect of fault type on the waveforms that are derived from the captured signals.

6.6.1 Single Phase to Earth Faults

A large number of 'a'-phase to earth faults have already been studied extensively in the previous sections. Figures 6.28 and 6.29 show the relay responses associated with modes 2 and 3 (ie. V_x and V_y) at end S for a 'c'-phase to earth fault. The fault is applied when the 'a'-phase voltage at bus S is passing through zero. These results demonstrate that there are no significant differences between the various waveforms for the single phase to earth fault as applied on different phases. The frequency spectra of the two modes show a slight variation, for example in case of mode V_x has more distortion, which is due to the different phase voltage combinations that are used to determine the modes and also effect of the signal clipping.



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

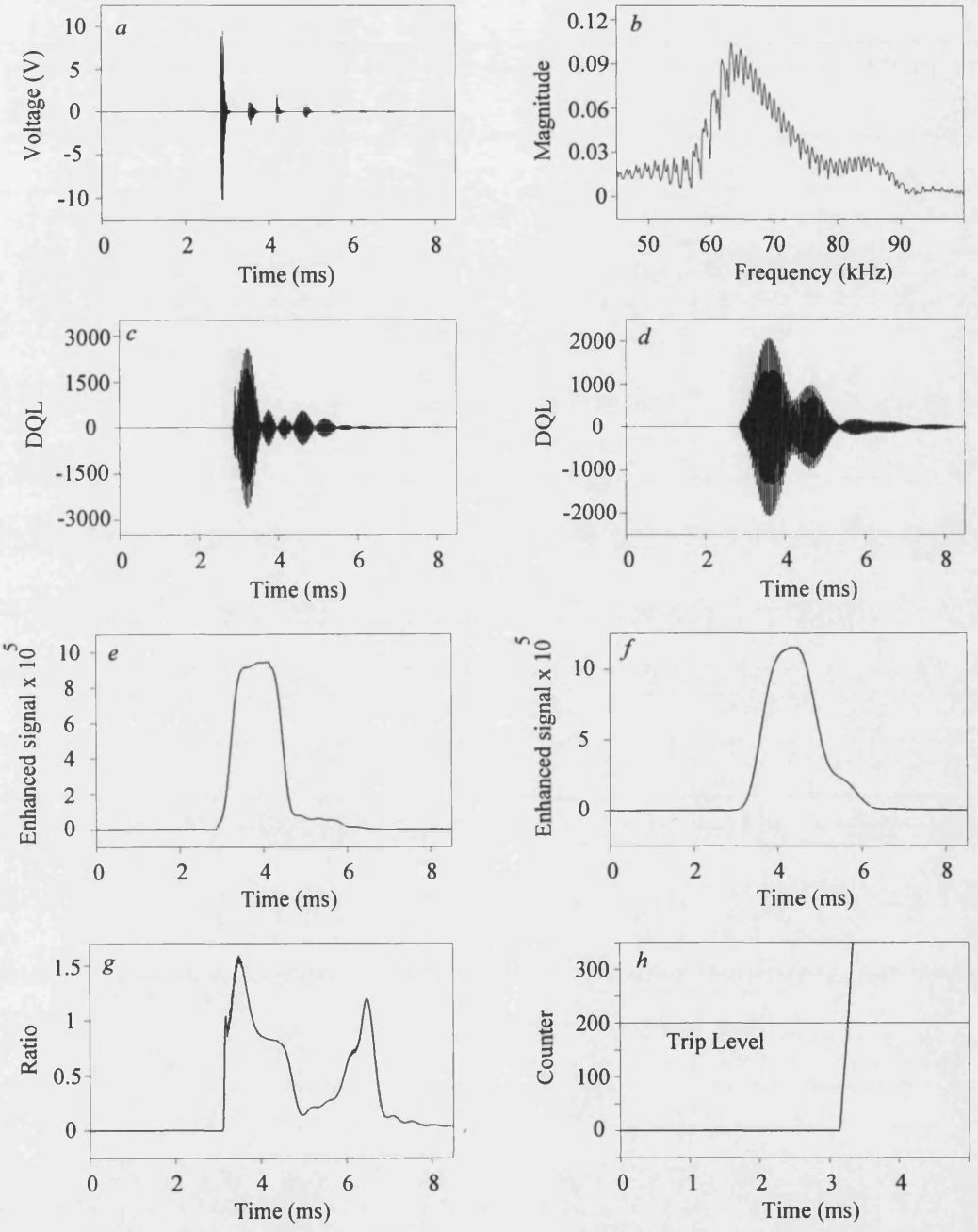
g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 6.28 Mode 2 relay response at end S for a C-E fault



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

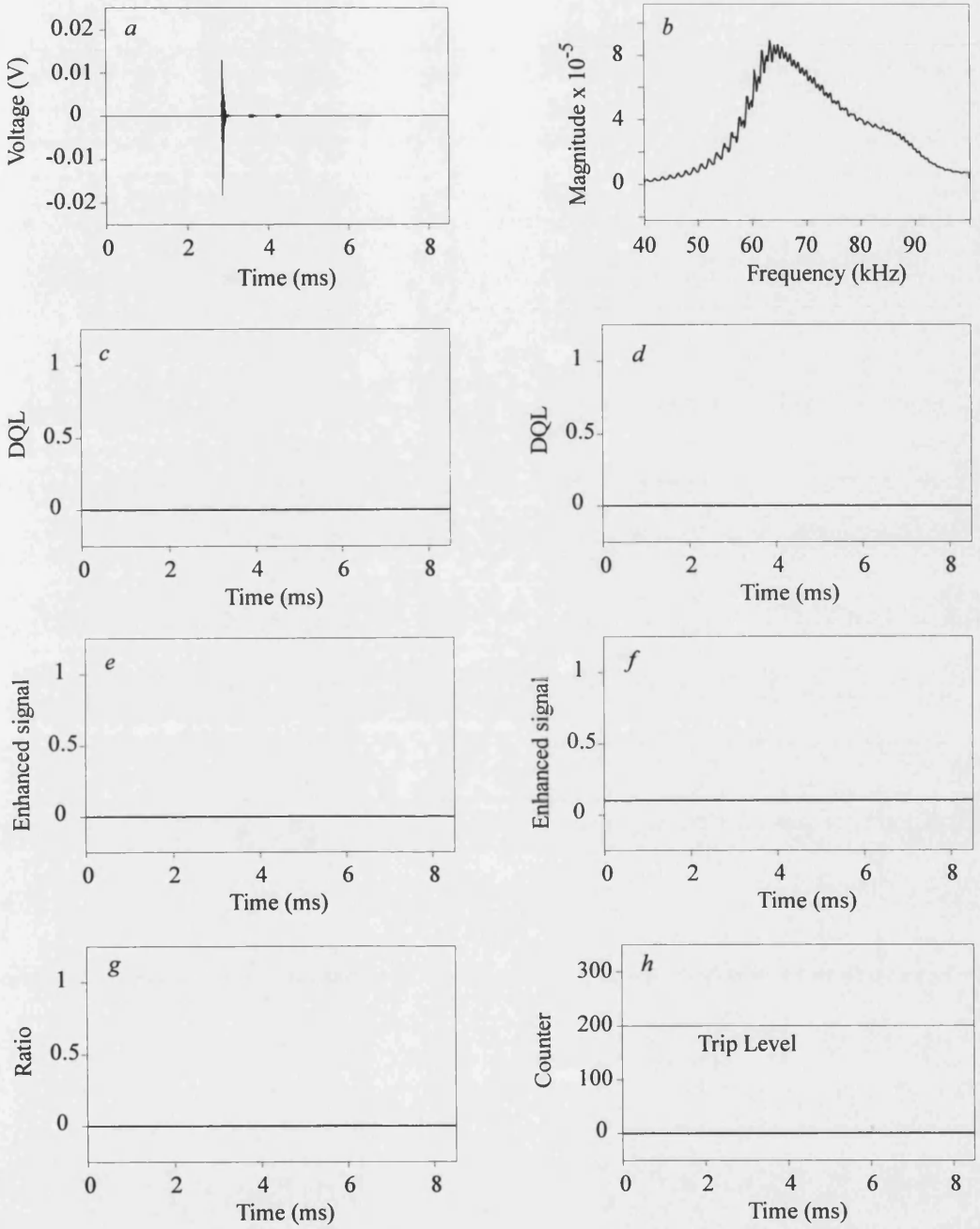
DQL = Digital quantum levels

Figure 6.29 Mode 3 relay response at end S for a C-E fault

6.6.2 Phase to Phase Faults

An 'a'-phase to 'c'-phase fault clear of ground is applied at a point when the voltage V_{ac} is passing through zero (ie. when the 'a'-phase voltage is passing through 30^0). For this type of fault, the aerial mode 2 signal ($V_x = V_a - 2V_b + V_c$) is virtually non-existent and this is so because the 'a'-phase voltage is nearly equal and opposite to the 'c'-phase voltage. The net effect is that the HF signals captured are of a very small magnitude as shown in Figure 6.30a. As they are below the minimum threshold level of the relay algorithm (20 mV), the digital output level of this signal falls below 65 quanta (assuming a 16-bit A/D converter); this digital output signal is thus forced to zero within the relay algorithm and both filter outputs are zero as can be seen from Figures 6.30c, d. However, during the signal enhancement process, the enhanced operate filter is maintained at zero and the enhanced restraint filter output is forced to 0.1, in order to avoid an overflow arising from the division by zero. The discrimination ratio, therefore, stays at zero and no trip decision is issued. As shown in Figure 6.31, the aerial mode 3 ($V_y = V_a - V_c$) covers this specific fault condition and correctly gives a trip output at end S in approximately 0.7 ms after fault inception.

A number of CAD studies were performed to simulate different phase to phase faults; the results showed that faults involving more than one phase always produce a relatively larger amount of HF components compared to single phase to ground faults. More importantly, the relay performance was always satisfactory both for internal and external faults.



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

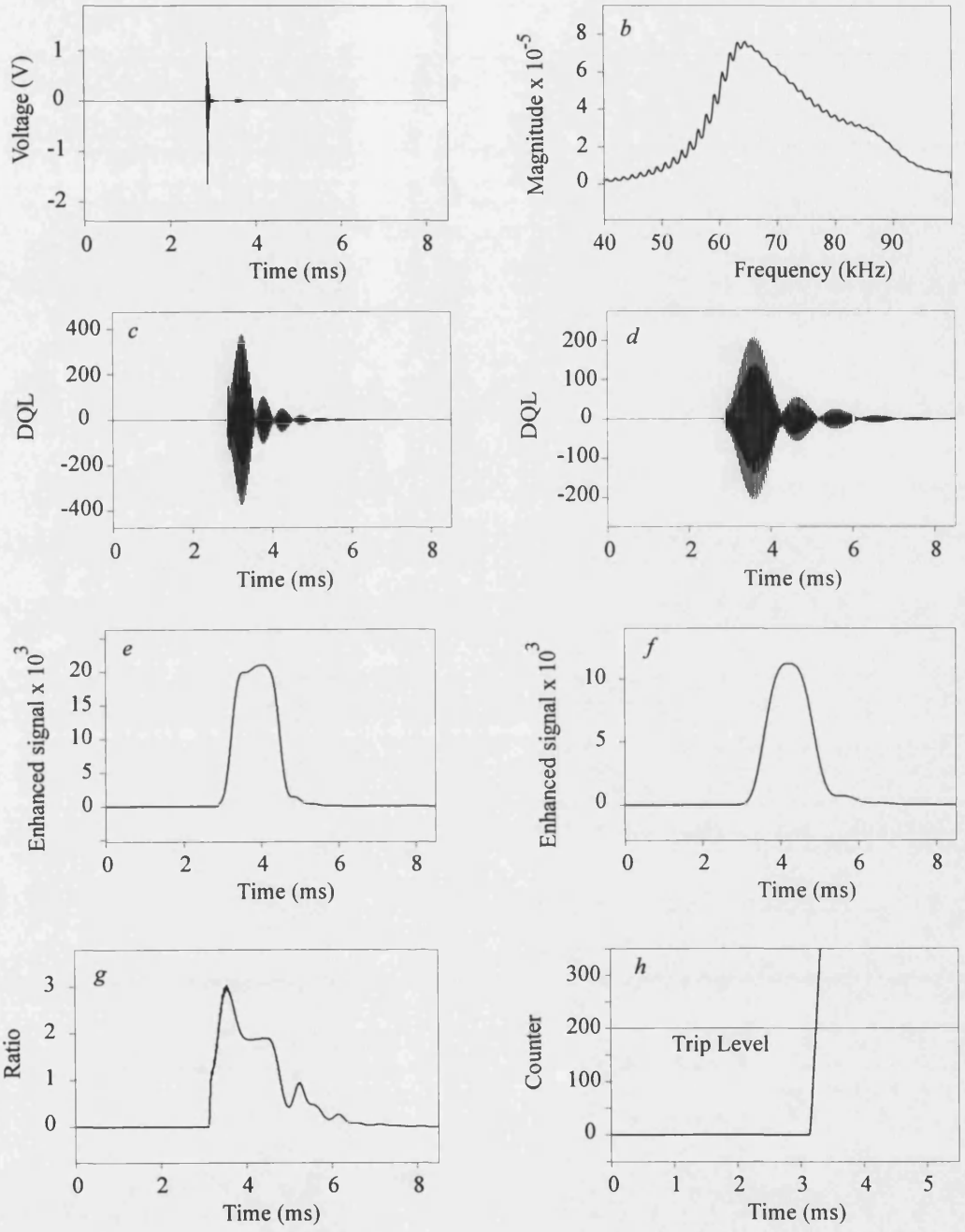
g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 6.30 Mode 2 relay response at end S for an A-C fault



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

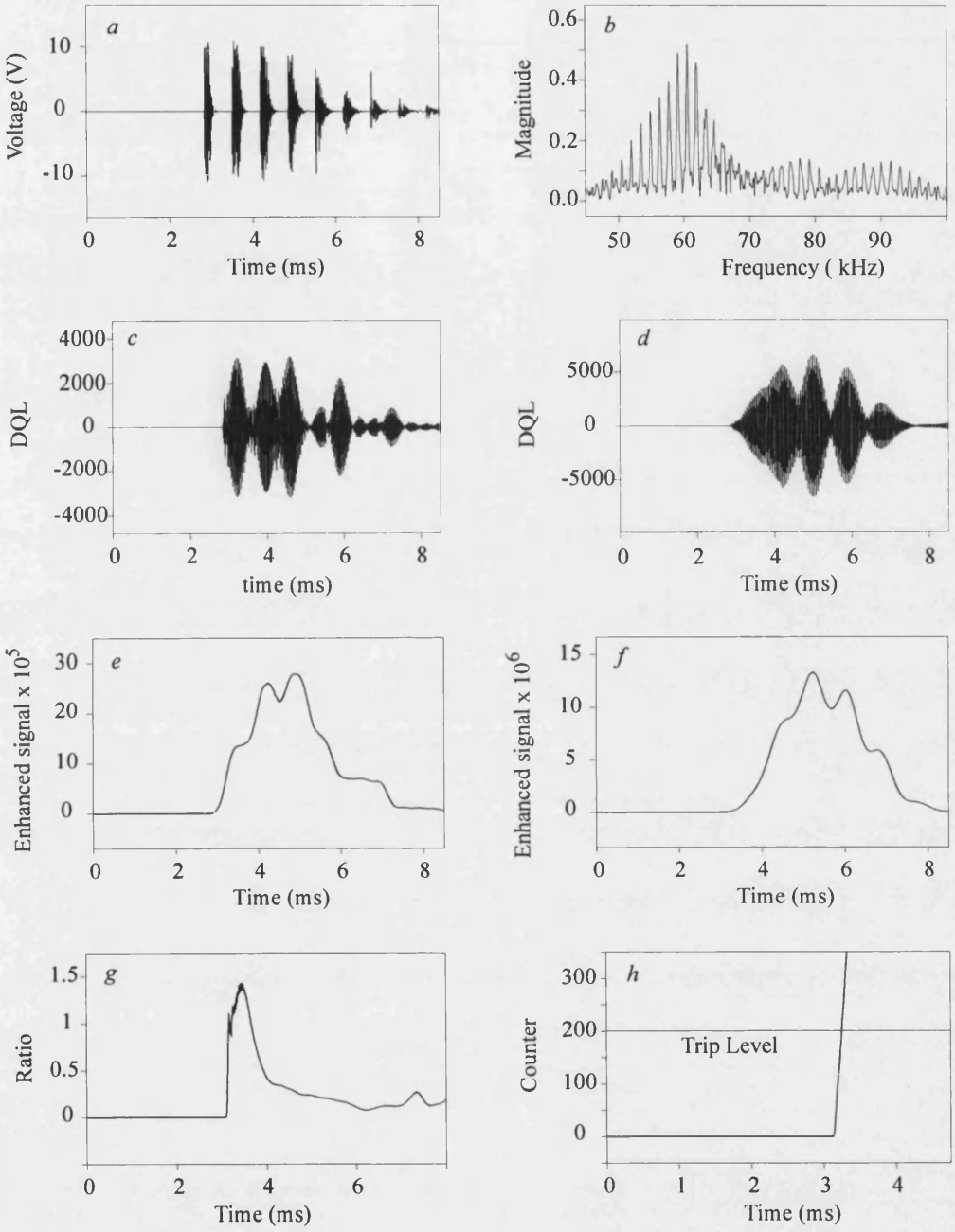
DQL = Digital quantum levels

Figure 6.31 Mode 3 relay response at end S for an A-C fault

6.6.3 Phase to Phase to Earth Faults

Figures 6.32 and 6.33 depict the response of modes 2 and 3 (V_x and V_y) respectively at end S following a 'b'-phase to 'c'-phase to earth fault at F_6, the fault resistance being approximately 1 Ω. The fault occurs when the 'a'-phase voltage is going through zero. As evident from Figure 6.32a and 6.33a, the magnitudes of the HF signals detected are relatively large in this case and this is because both the faulted phase voltages contribute to the HF components. The enhanced filter outputs are very large due to the effect of the moving average algorithm, as evident from Figures 6.32e, f, and 6.33e, f. For this type of fault, both the aerial modes are active and give a trip decision in just under 0.75 ms after fault inception.

Although not shown here, the relay performance is stable for phase to phase to earth faults occurring outside the protected zone.



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

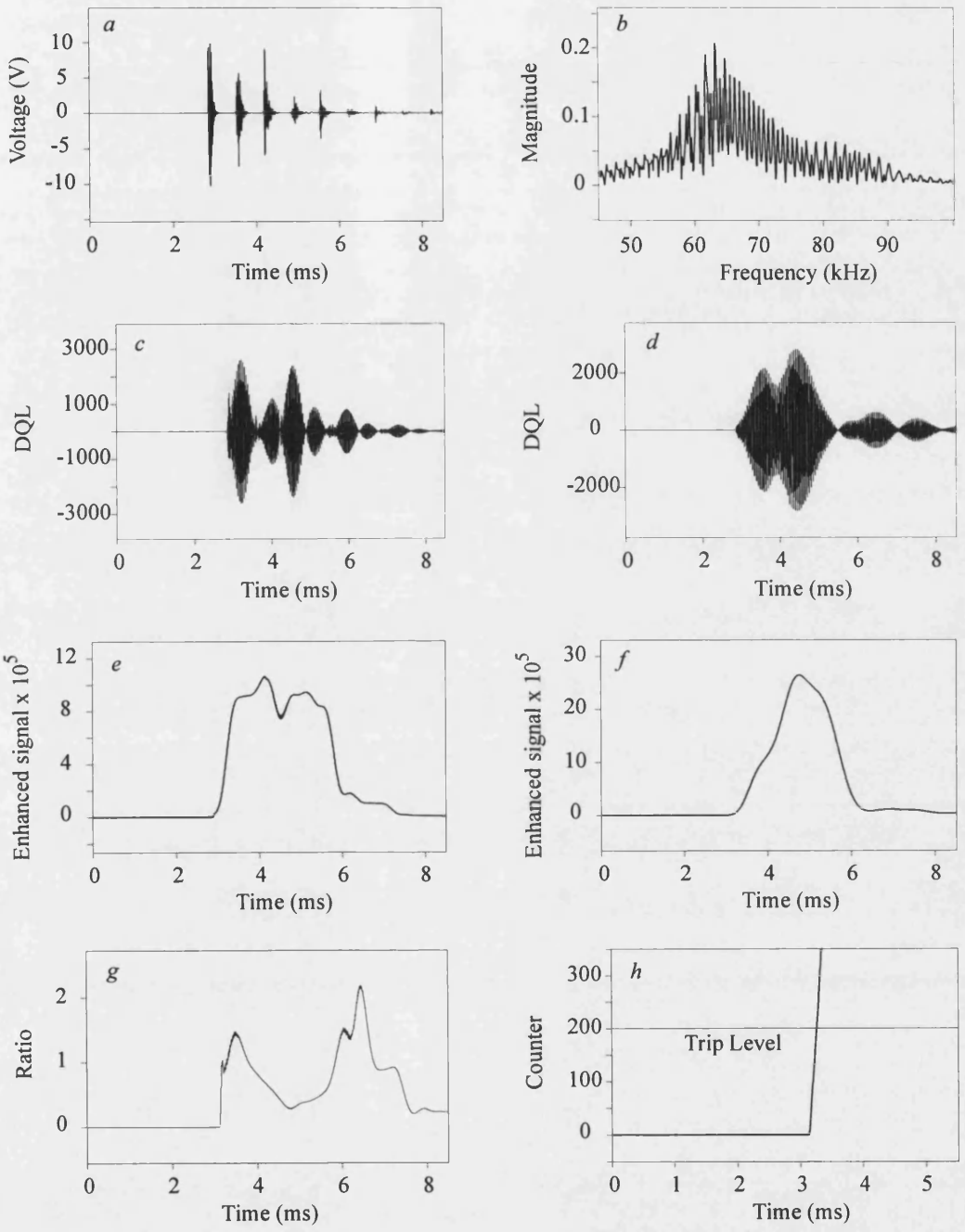
g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 6.32 Mode 2 relay response at end S for a B-C-E fault



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

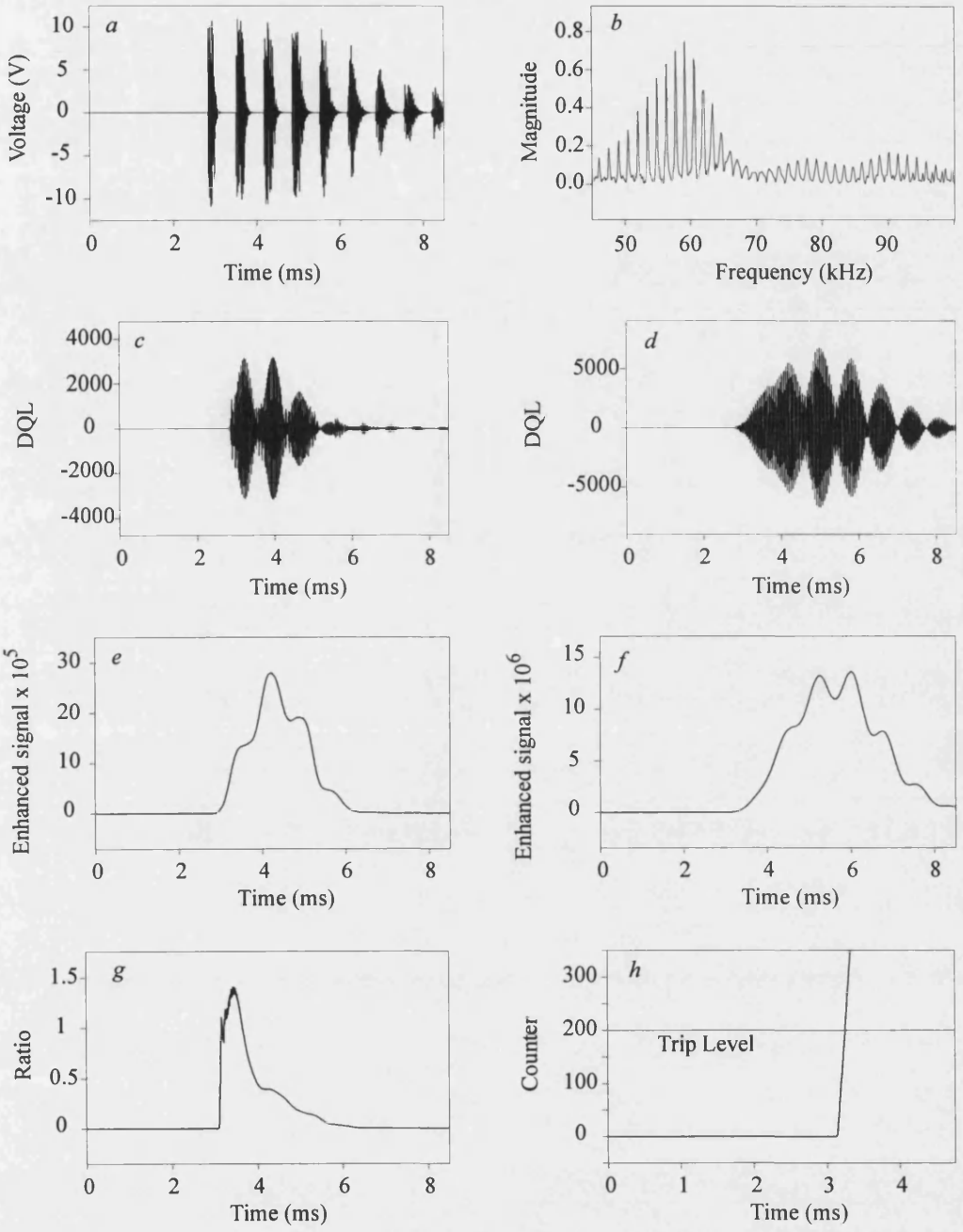
DQL = Digital quantum levels

Figure 6.33 Mode 3 relay response at end S for a B-C-E fault

6.6.4 Three Phase Faults

In general, three phase faults clear of ground are considered to be the most severe type encountered on a power system; however, they are the least common. Figures 6.34 and 6.35 typify the modes 2 and 3 (V_x and V_y) waveforms at end S for a three phase fault clear of ground again at F_6. The fault is again applied when the 'a'-phase voltage is passing through zero. The considerable energy in the initial HF bursts can be particularly seen with the mode 2 signal (Figure 6.34a). Many of the subsequent reflections are clipped by the limiter and the frequency spectrum shows a significant amount of energy around 60 kHz (Figure 6.34b). The enhanced filter outputs reach very high values as the components of the individual reflections are averaged together (Figures 6.34e, f). However, the trip decision is reached at end S after approximately 0.76 ms following fault inception.

It should be noted that the signal detected by mode 3 signal (V_y) is lower than for mode 2 (V_x) and this as a direct consequence of their modal voltage compositions (Figures 6.35a). Again a trip decision is given in just under 0.77 ms.



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

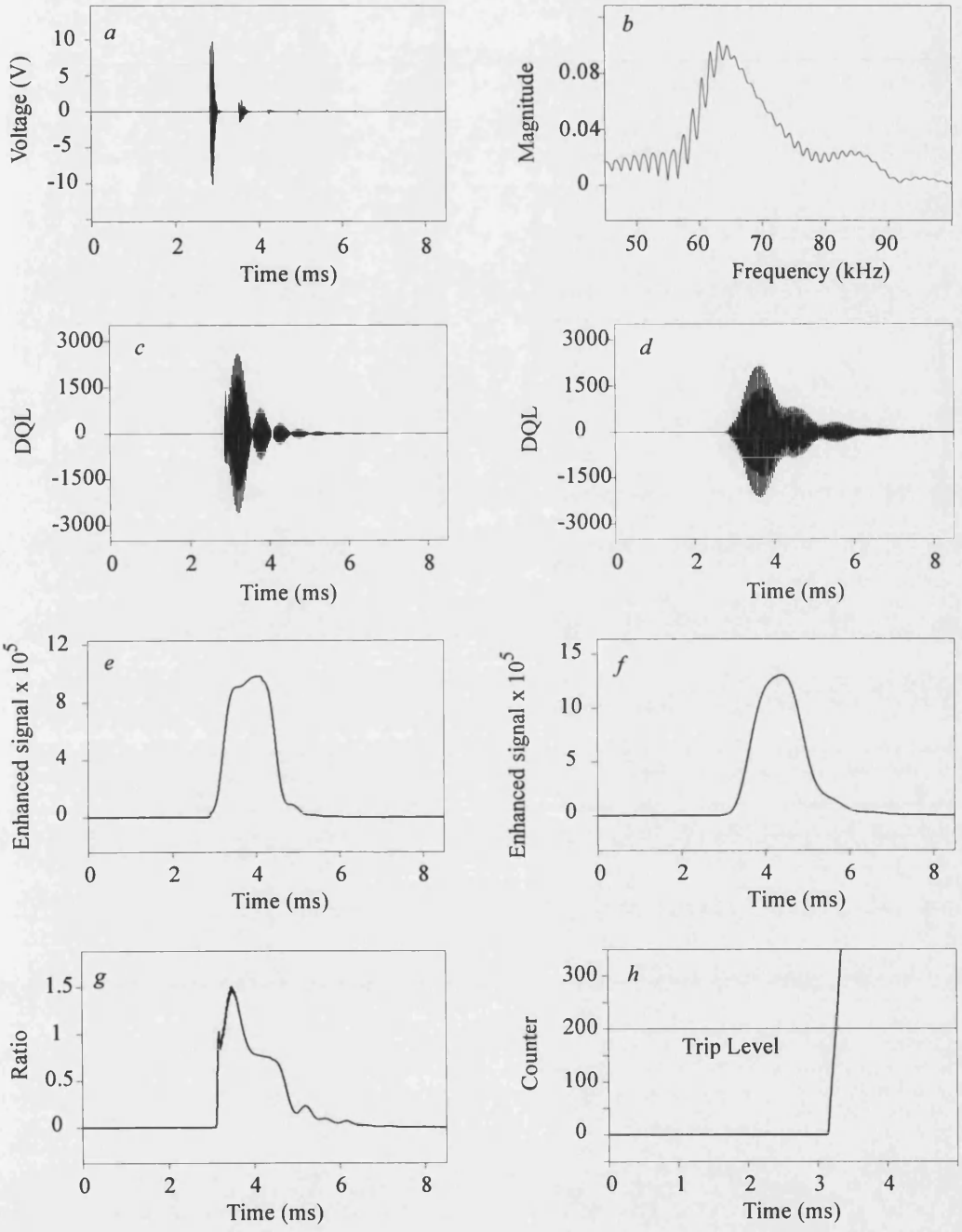
g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 6.34 Mode 2 relay response at end S for an A-B-C fault



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

g Discrimination ratio

h Trip counter output

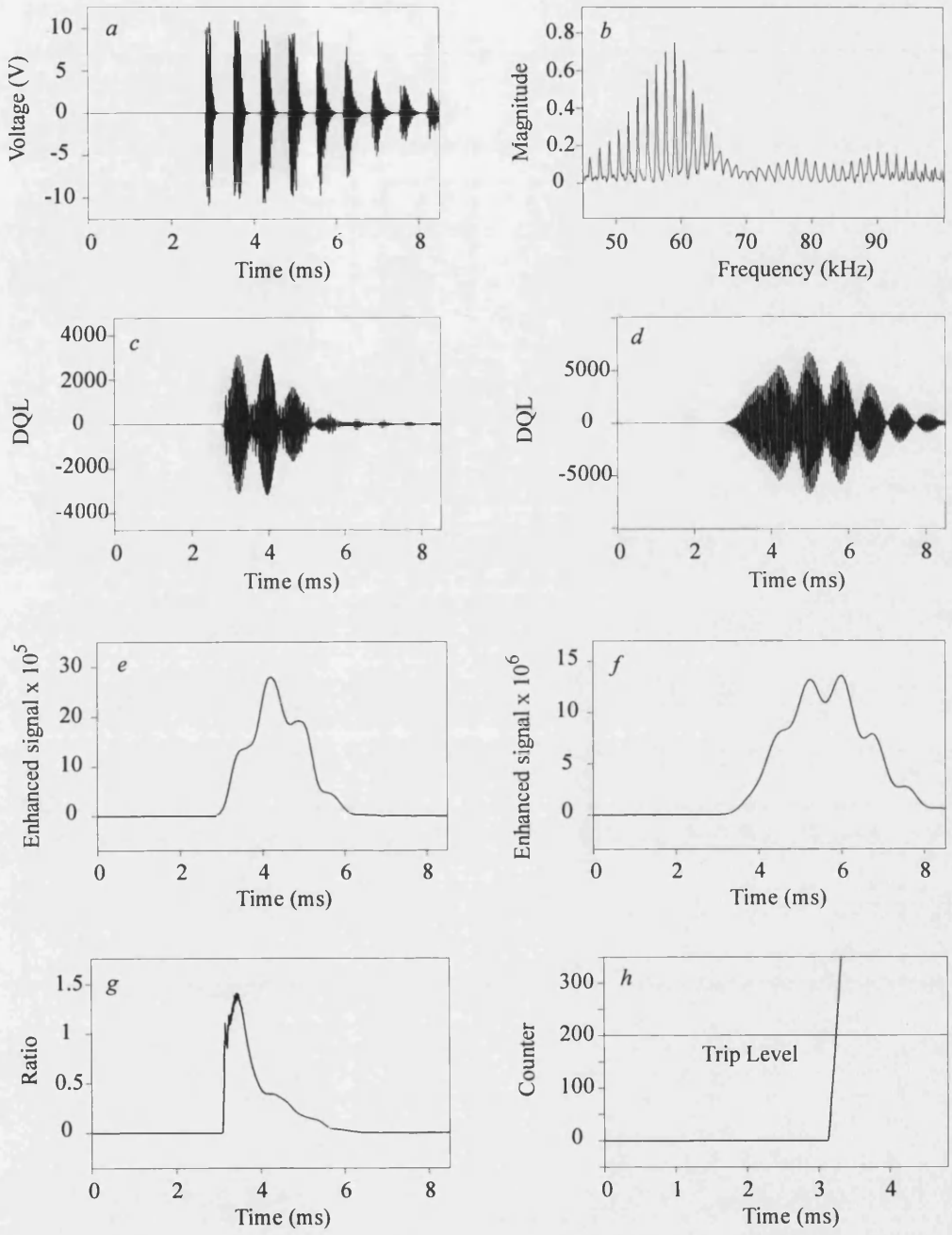
Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 6.35 Mode 3 relay response at end S for an A-B-C fault

6.6.5 Three Phase to Earth Faults

Figures 6.36 and 6.37 show the modes 2 and 3 (V_x and V_y) waveforms at end S for a three phase to earth fault; again the fault is applied when the 'a'-phase voltage is passing through zero. There are no major differences between the waveforms for a three fault and a three phase to earth fault; this is somewhat expected because for all intents and purposes, both these faults are balanced in nature. Very large quantities of HF signals are detected in this case because all the three phase voltages are reduced to earth potential. The trip decisions are given in approximately 0.75 ms and 0.78 ms for modes 2 and 3, respectively at end S.



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

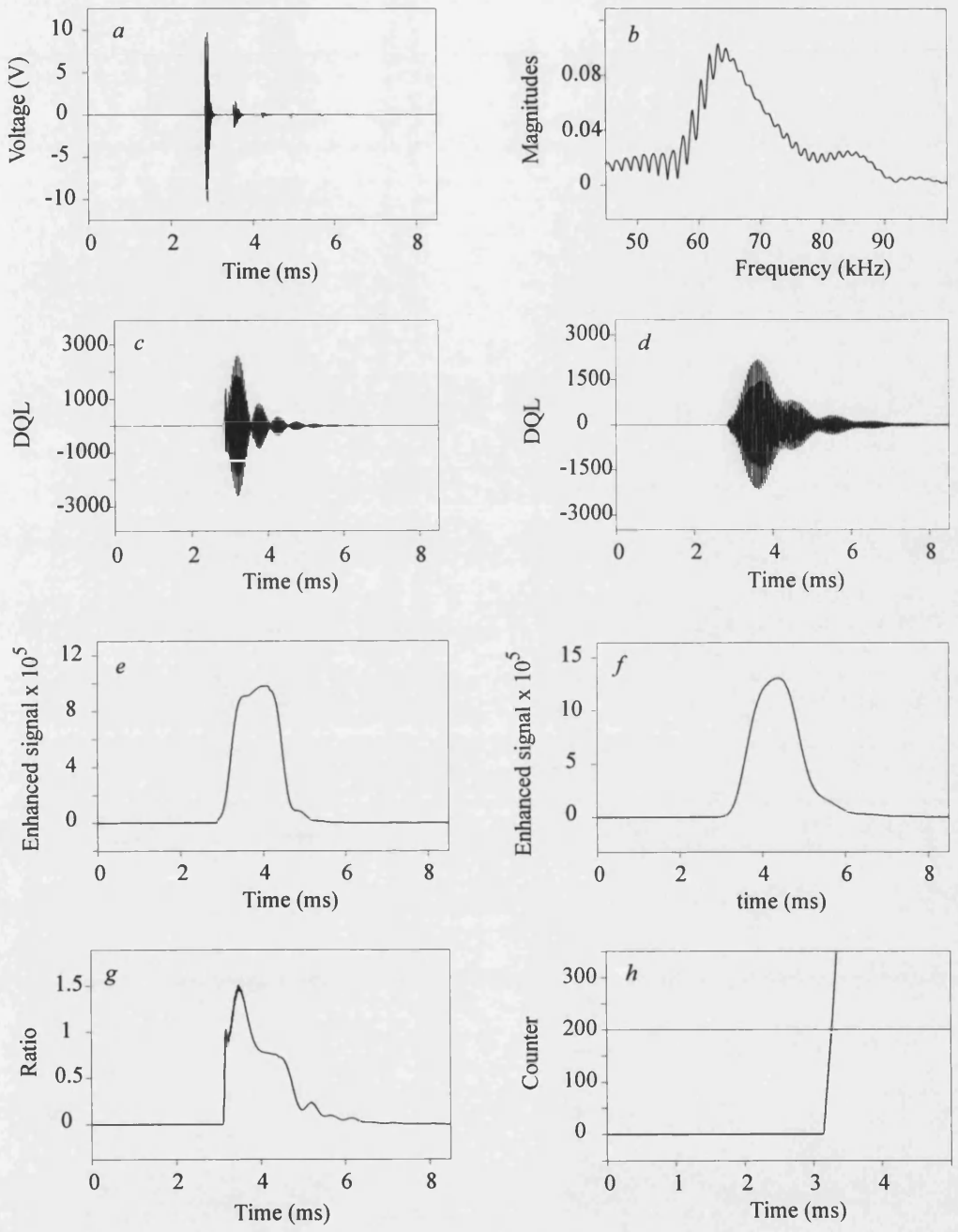
g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 6.36 Mode 2 relay response at end S for an A-B-C-E fault



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

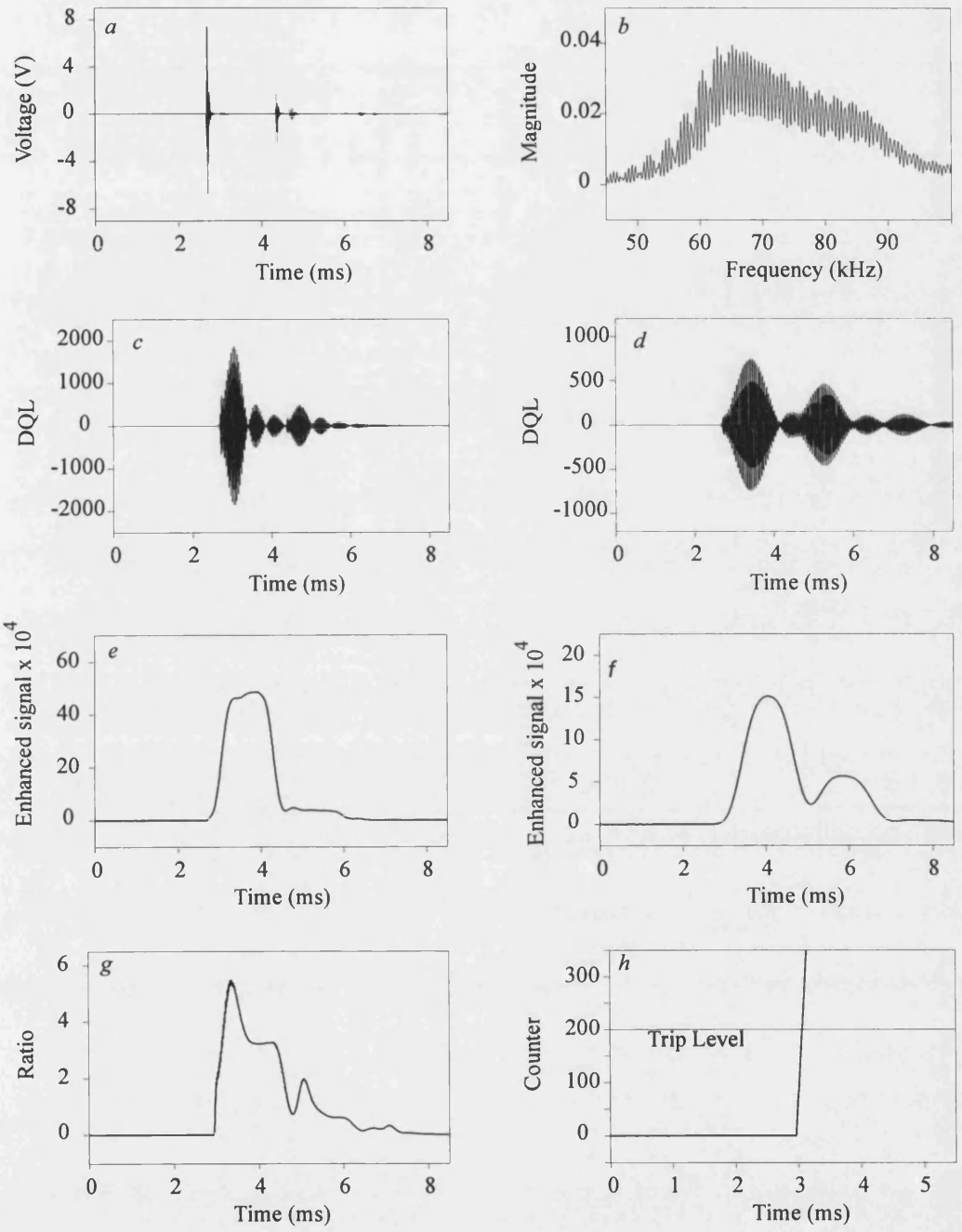
DQL = Digital quantum levels

Figure 6.37 Mode 3 relay response at end S for an A-B-C-E fault

6.7 Relay Performance Under High Impedance Faults

In practice, although over 90% of faults in power transmission systems are low impedance arcing faults, other types of faults do occur, for example non-arcing permanent faults, involving high resistance. It is thus important to test the new relay scheme for such faults. Figures 6.38-6.40 show the mode 2 (V_x) relay response for an 'a'-phase to earth non-arcing fault involving fault resistances of 50 Ω, 150 Ω and 300 Ω, respectively. The faults are applied when the 'a'-phase voltage is passing through 10^0, and the fault is at 50 km from the end S, at F_3 in Figure 4.2a; again MOV scheme is employed.

As expected, although the magnitudes of the HF signal are attenuated by the increase in the fault resistance (Figures 6.38a-6.40a), this has little bearing on the performance of the protective relay, as clearly evident from the relay performance shown in Figures 6.38-6.40. There is hardly any difference in the discrimination ratios recorded at end S as it is calculated using a comparison of the amount of energy in the specific frequency bands and not their actual magnitudes. It should be noted that in the absence of fault arcs, the HF phenomenon is due to the travelling wave effect. A series of CAD studies has shown that, although the relay can theoretically detect faults involving resistances well above 500 Ω, in practice the upper limit of tolerance is likely to depend heavily on the levels of spurious noise induced in the electronic circuitry in the hostile environment of a substation.



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

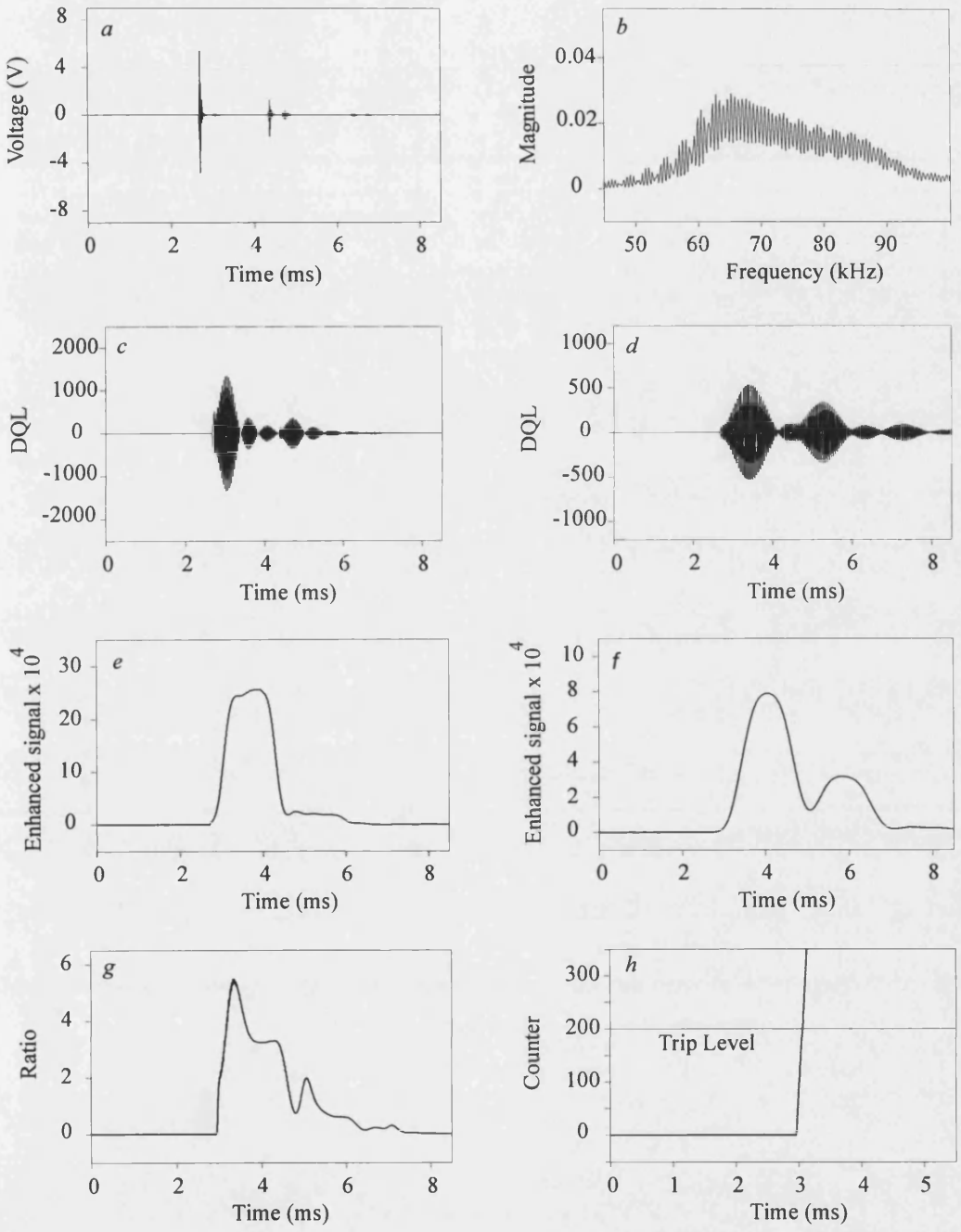
g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 6.38 Mode 2 relay response at end S for a high impedance fault with 50Ω fault resistance



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

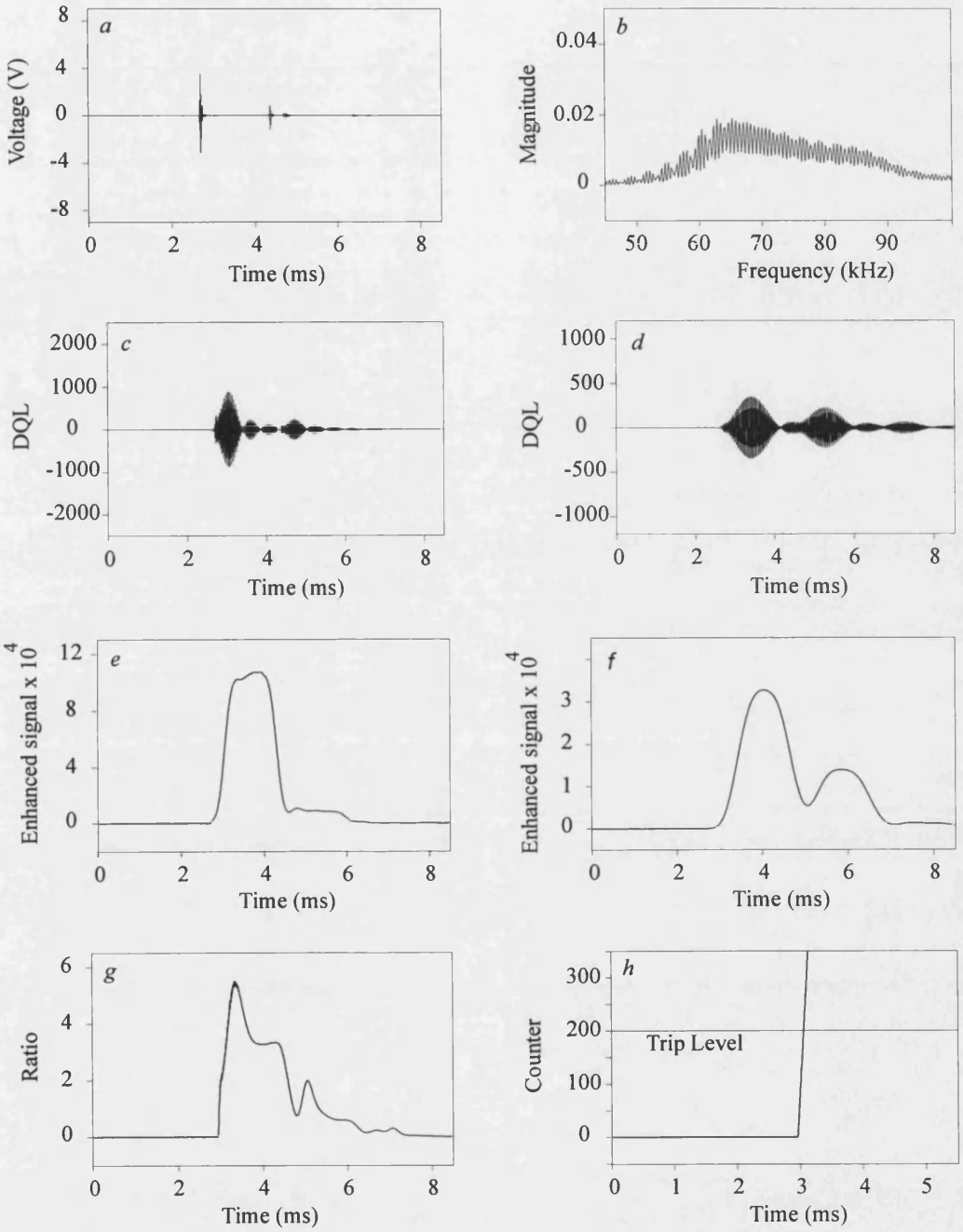
g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 6.39 Mode 2 relay response at end S for a high impedance fault with 150Ω fault resistance



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

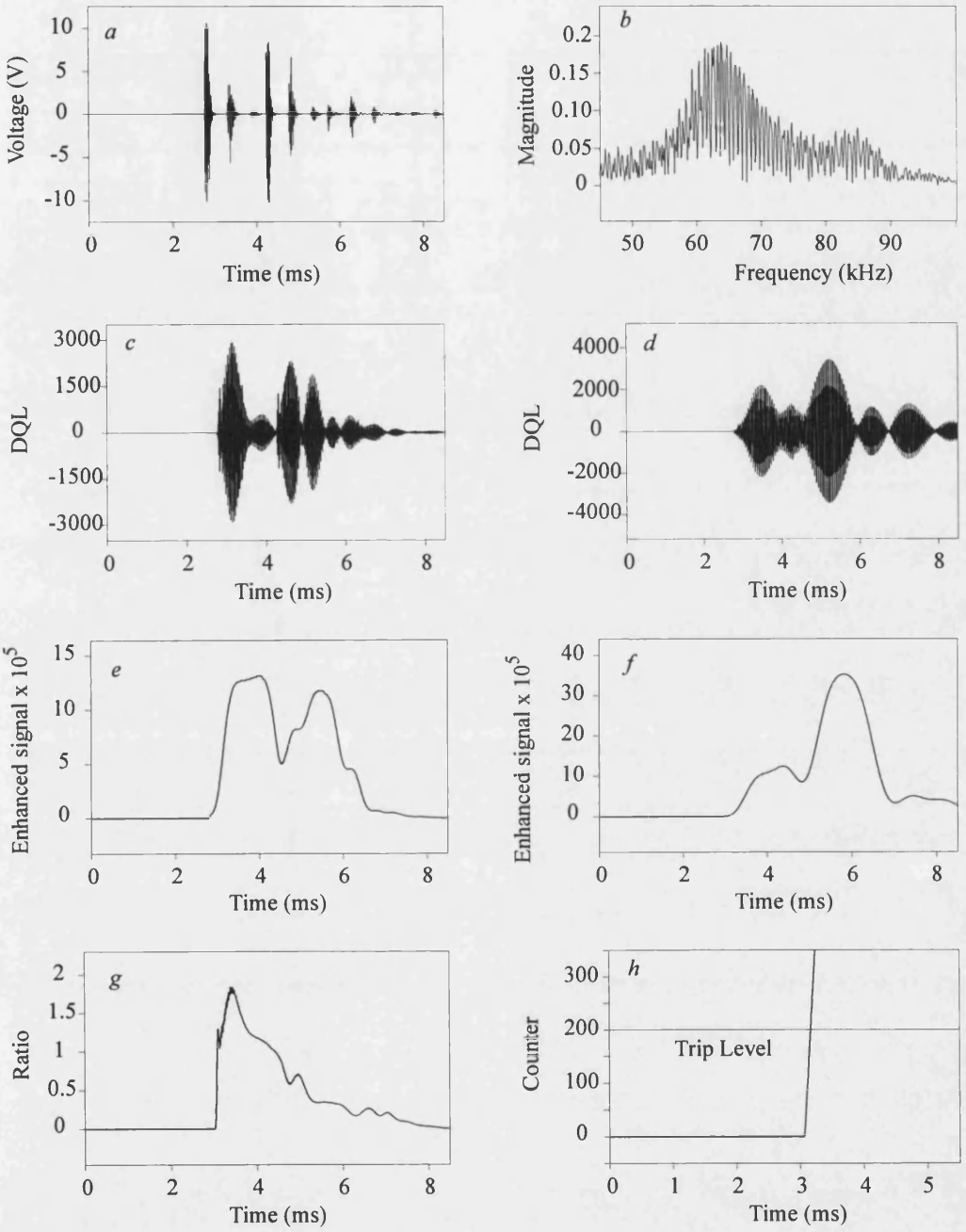
DQL = Digital quantum levels

Figure 6.40 Mode 2 relay response at end S for a high impedance with 300Ω fault resistance

6.8 Effect due to System Condition/Configuration Changes

6.8.1 Effect of Source Capacity Variations

The source parameters, particular their capacities, can change from one time of the day to the other and can significantly affect the fault transient waveforms. Thus, it is vitally important to verify the effect of source capacity variations on the performance of the proposed relay scheme. In this study, this is achieved by changing the source capacities of the single section feeder system of Figure 4.2a to 40 GVA and 5 GVA at end S and R respectively and then applying a voltage maximum 'a'-phase to earth fault at F_1 . Comparing the end S and R mode 2 (V_x) waveforms (Figures 6.41, 6.42) to the corresponding results with source capacities of 20 GVA and 0.5 GVA at end S and R (Figures 6.13, 6.14) respectively, it can be seen that there is very little visible difference between them; more importantly, the relay performance attained in the two cases is hardly changed. This is so because, the protected zone is effectively bounded by the combined terminating busbar capacitances and the line trap units which form a strong barrier between the protected line and the source side network. Thus, the performance of this relay scheme is largely independent of the source side network configurations and generating capacities.



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

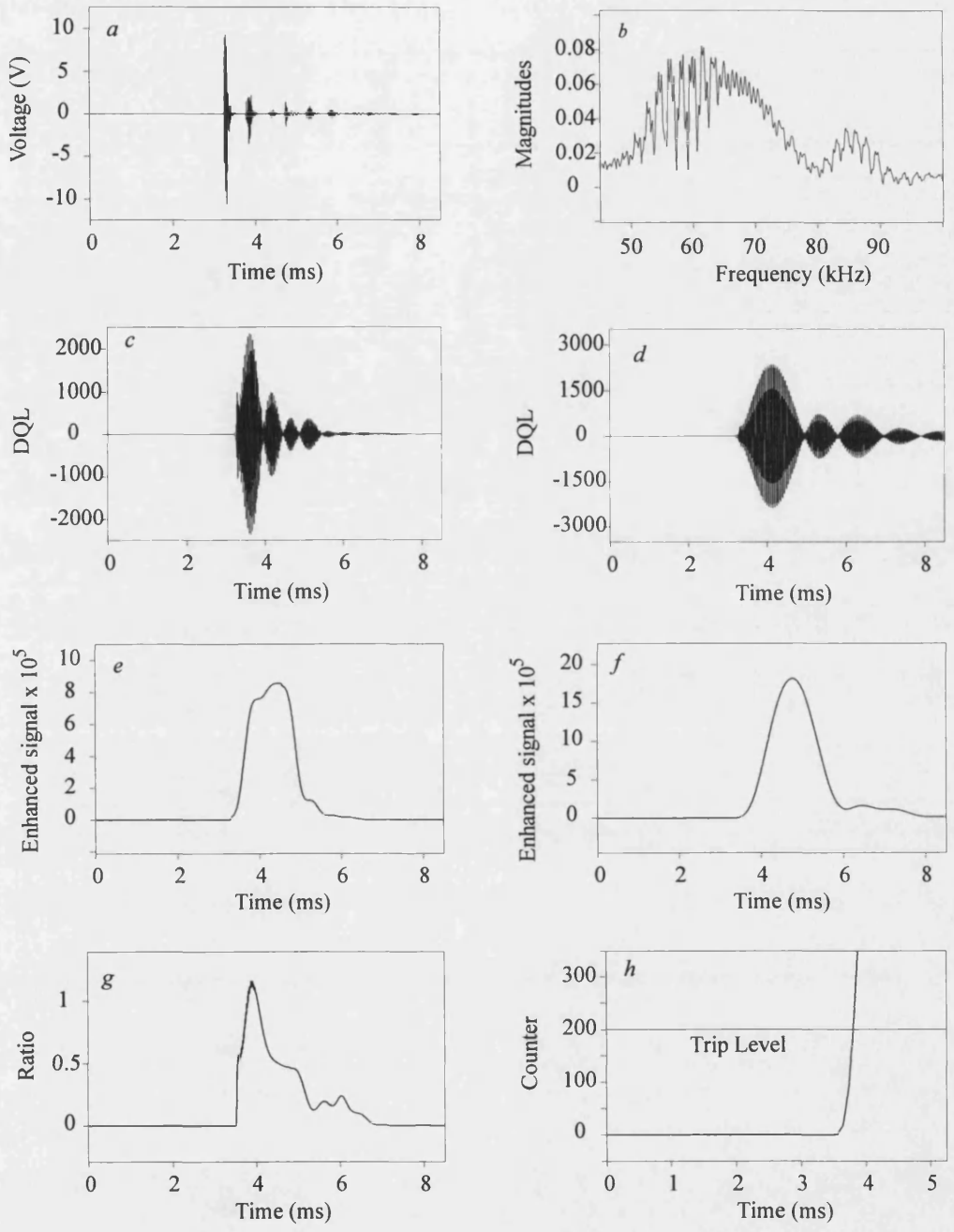
g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 6.41 Effect of source capacity variation at end S relay



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

g Discrimination ratio

h Trip counter output

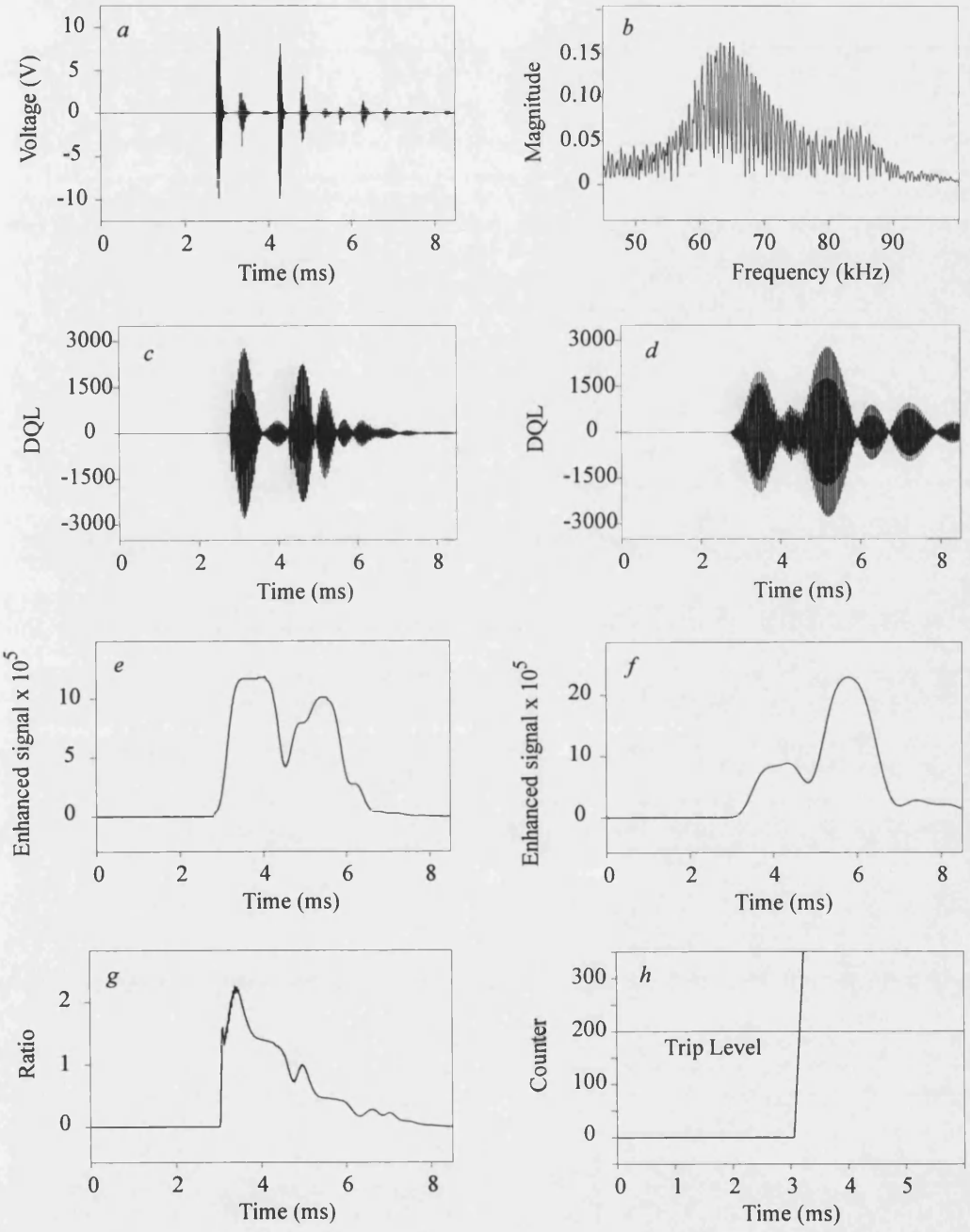
Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 6.42 Effect of source capacity variation at end R relay

6.8.2 Effect of Line Loading

Figure 6.43 and 6.44 show the effect of prefault loading of the transmission lines when an 'a'-phase to earth fault is applied at 45^0 on the system of Figure 4.2a at F_1. In this particular fault case, the phase angles of the source voltages at end R are shifted by -10^0 relative to the source voltages at end S. Here again, there are only very minor differences between the relay response compared to that obtained when there is no power transfer (Figures 6.10, 6.11).



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

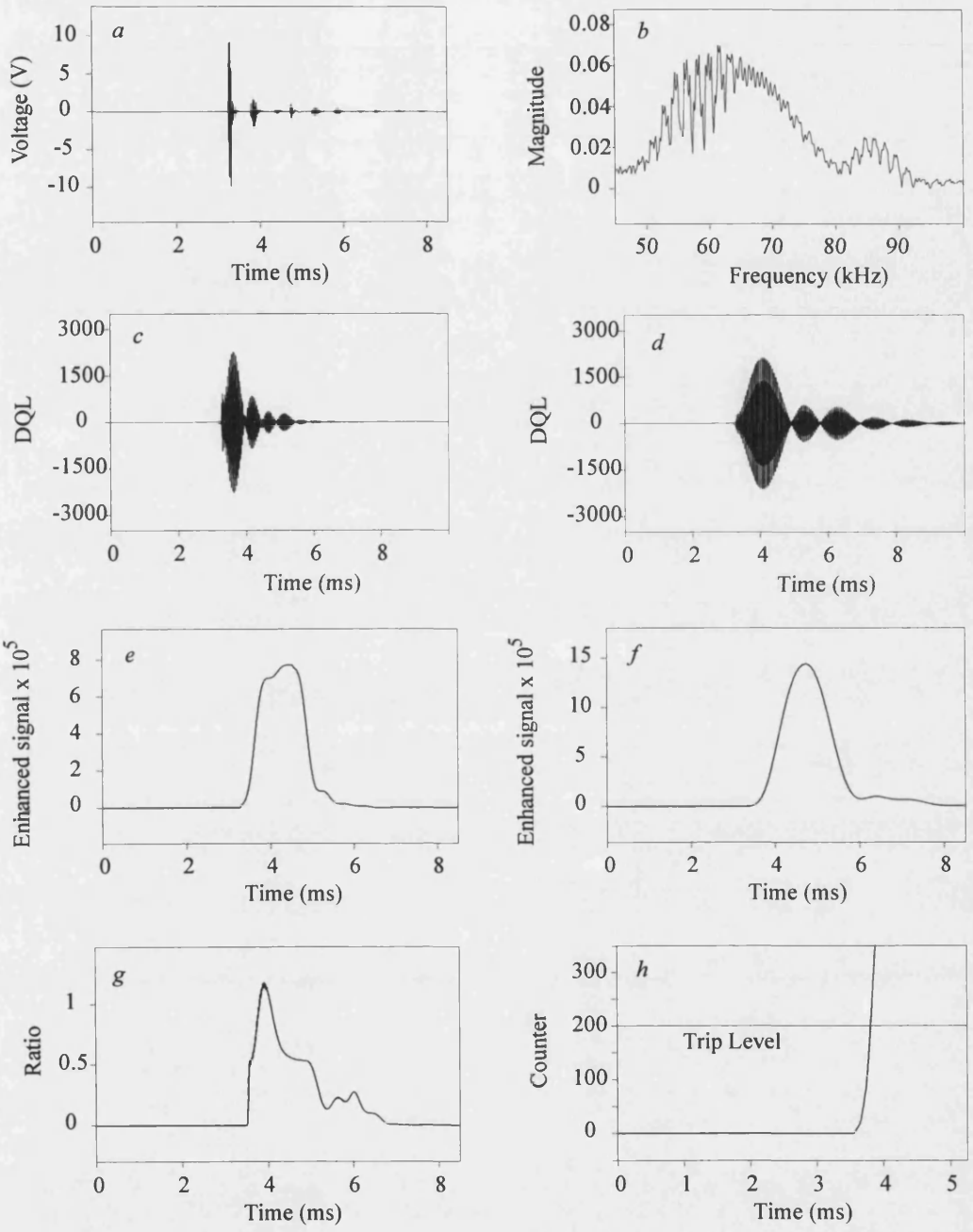
g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 6.43 Effect of line loading at end S relay



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

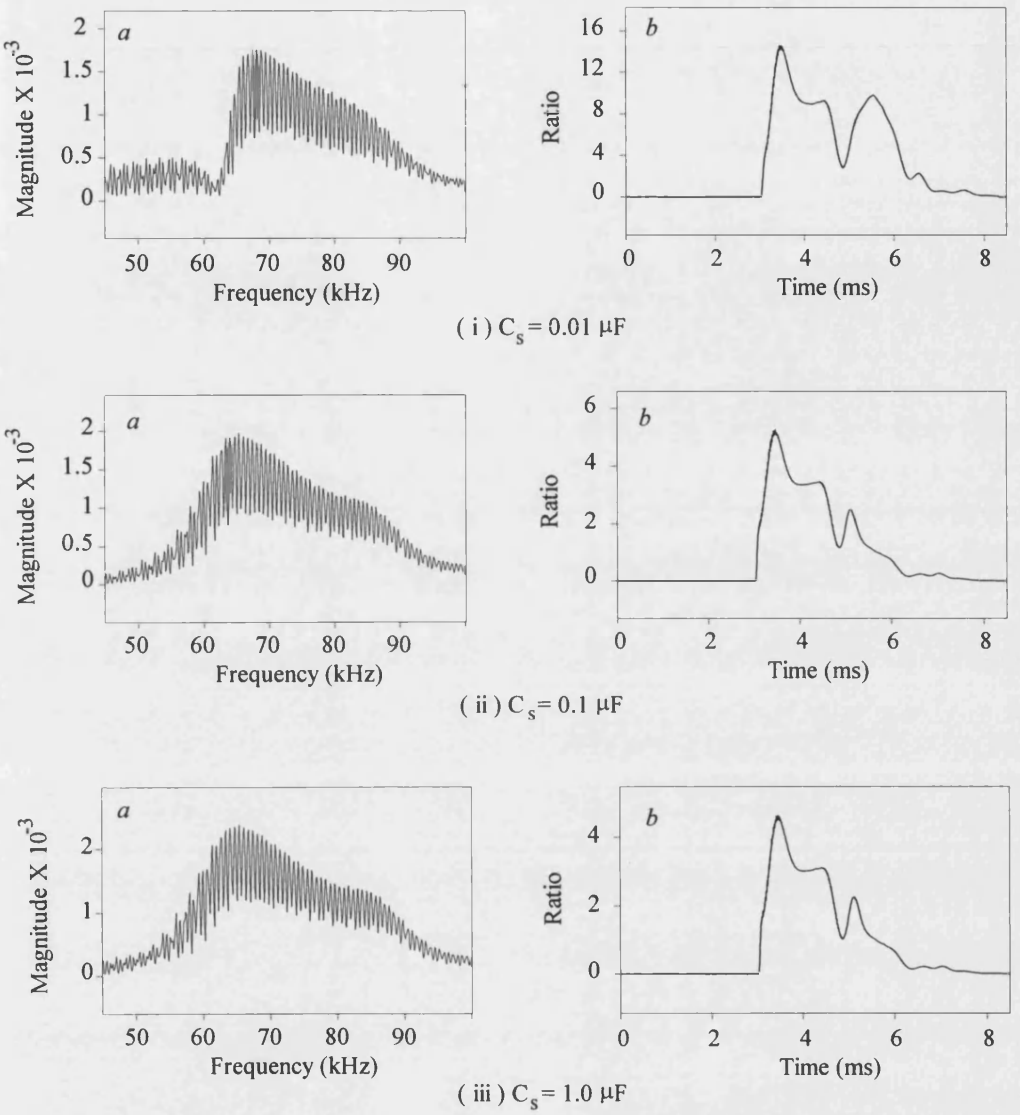
DQL = Digital quantum levels

Figure 6.44 Effect of line loading at end R relay

6.8.3 Effect of Bus-bar Capacitance

The busbar capacitance employed in all studies presented in this thesis is 0.1 μF which is very typical of that encountered in practice. However, depending on the busbar arrangement in a particular substation, it could be quite different in certain system configurations. The sensitivity of the scheme to changes in the values of the busbar capacitance are examined by altering C_S at both end S and R, in Figures 4.2a, from 0.01 μF to 1 μF. Figure 6.45 shows the frequency spectra of HF signals attained and the discrimination ratios of mode 2 (V_x) at end S for the internal fault near voltage zero (at F_1 in Figure 4.2a). When the value of the busbar capacitance is 0.01μF the discrimination ratio is significantly greater than unity as shown Figure 6.45(i)b; this is so because the spectral energy content of the signal at the lower restraint frequency (60 kHz) is much less than that at the higher operate frequency (75 kHz) as evident from Figure 6.45(i)a.

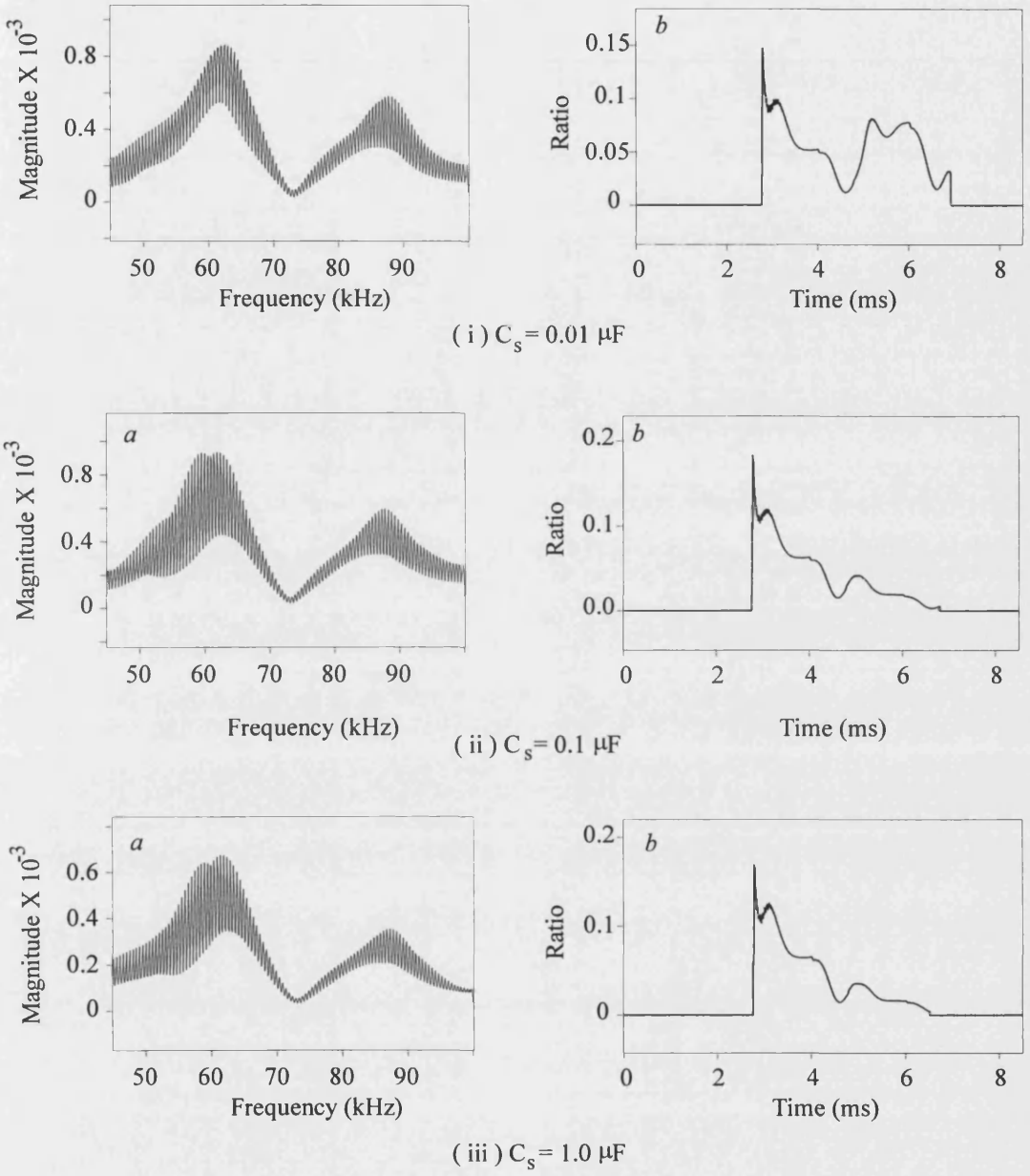
Figure 6.46 shows the frequency spectra of HF signals attained and corresponding discrimination ratios of mode 2 signal (V_x) at end S for the external voltage zero fault (at F_2 in Figure 4.2a). It is apparent that the frequency components in the two bands of interest are only marginally affected and the results attained clearly show that these small changes have no detrimental effect on the relay stability for the external faults, (ie. the discrimination ratio stays well below unity) as evident from Figure 4.46b.



a Mode 2 (V_x) frequency spectra at end S

b Mode 2 (V_x) discrimination ratios at end S

Figure 6.45 Effect of varying busbar capacitance for internal fault



a Mode 2 (V_x) frequency spectra at end S

b Mode 2 (V_x) discrimination ratios at end S

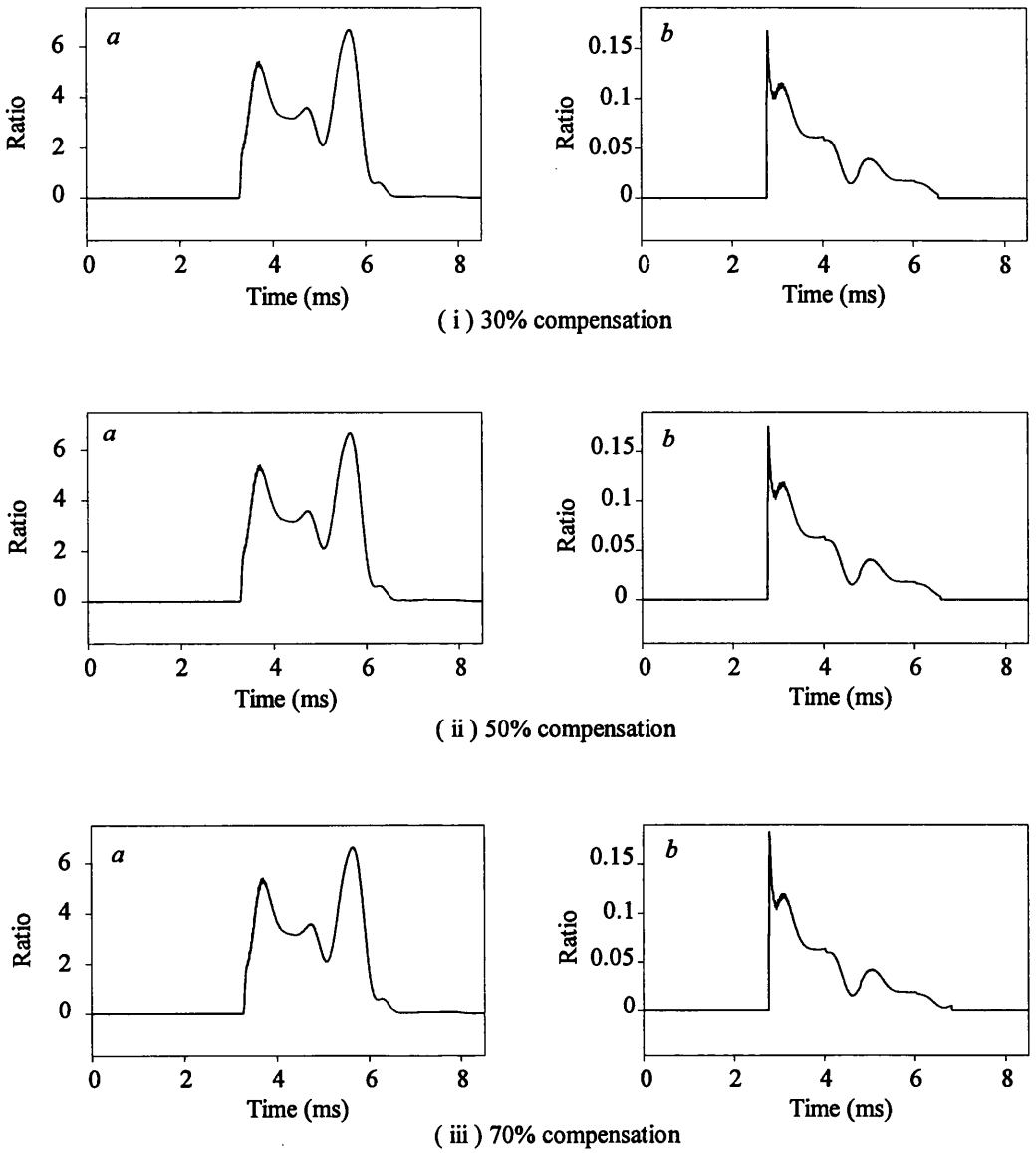
Figure 6.46 Effect of varying busbar capacitance for external fault

6.8.4 Effect of Circuit Configuration

All the results presented sofar in this chapter are obtained from the digital simulation models of series compensated systems with a typical level of compensation of 70%, the compensation being provided near the line ends. The performance of the scheme for different circuit configurations is best demonstrated by applying a variety of faults to the network of Figures 4.2, with different levels of compensation at both line ends and at the midpoint.

6.8.4.1 Effect of Degree of Series Compensation

In order to see the effect of degree of series compensation on the relay performance, 'a'-phase to earth internal and external faults are applied at 45^0 with respect to the 'a'-phase on the system of Figure 4.2a at F_4 (150 km from end S) and F_2 (just behind the line trap) respectively; the degree of compensation is changed from 30% to 70%. Figure 6.47 shows that the ratio of the discriminant signals is always maintained at well above unity for the internal fault and, for the external faults, the ratio of the discriminant signals is very small (close to zero), and there is very little visible difference between each set of waveforms as the level of compensation is changed. It should be noted that, because the new relay technique utilises HF components well removed from the power frequency, the performance is largely independent of the circuit parameter such as degree of series compensation; this is so because the series capacitor virtually acts as a short circuit to the HF components of interest.



a Mode 2 (V_x) discrimination ratios at end S for internal fault

b Mode 2 (V_x) discrimination ratios at end S for external fault

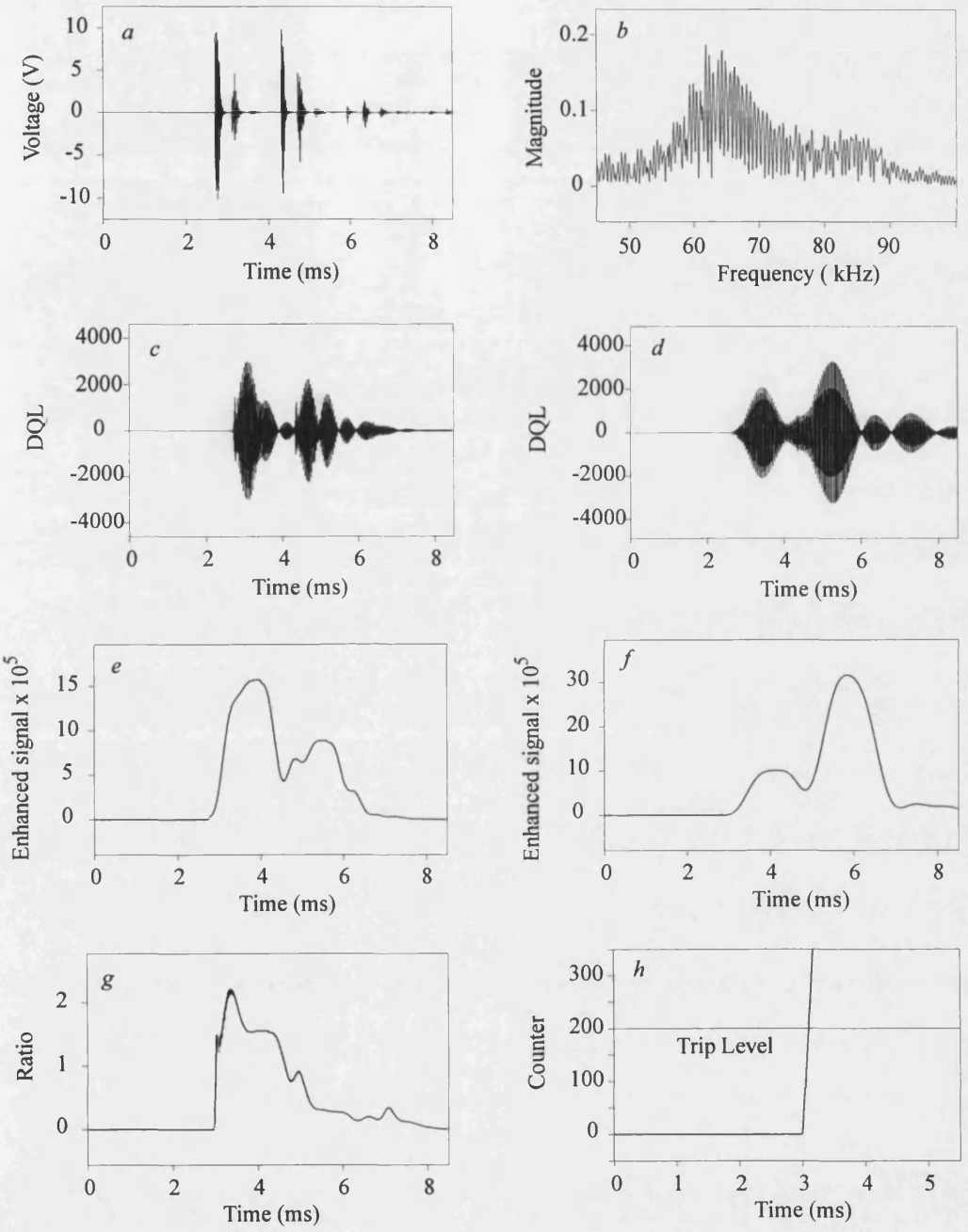
Figure 6.47 Effect of varying degree of series compensation

6.8.4.2 Compensation at Middle of the Line

In this section, the performance of the new relay is evaluated for the system where a single capacitor bank is located at the middle of the line with a typical level of compensation of 50%. Figures 6.48 and 6.49 typify the mode 2 (V_x) signal response at ends S and R, respectively for an 'a'-phase to earth fault with the MOV capacitor protective scheme. The fault is applied when the a-phase voltage is passing through 60^0, and the fault is at 60 km from end S and at point F_{10} on the multi-section system in Figure 4.2c.

HF signals of large magnitudes are generated for this particular fault and hence, the signal clipping action can be seen at both end relays, as shown in Figures 6.48a and 6.49a. The magnitudes of the signals received at each end are determined by the distance between the fault and the measurement equipment. The end R signals are attenuated as they travel the furthest distance. This means that they are clipped less and so there is lower distortion in the signals entering the end R protection relay. This can be clearly seen by comparing the frequency spectra and filter outputs at both line ends (Figures 6.48b-d, 6.49b-d).

However, the discrimination ratios at both line ends exceed one, less than a millisecond after fault inception. As far as the relay performance is concerned, results have shown that there are no major differences between the line end compensation and midpoint compensation.



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

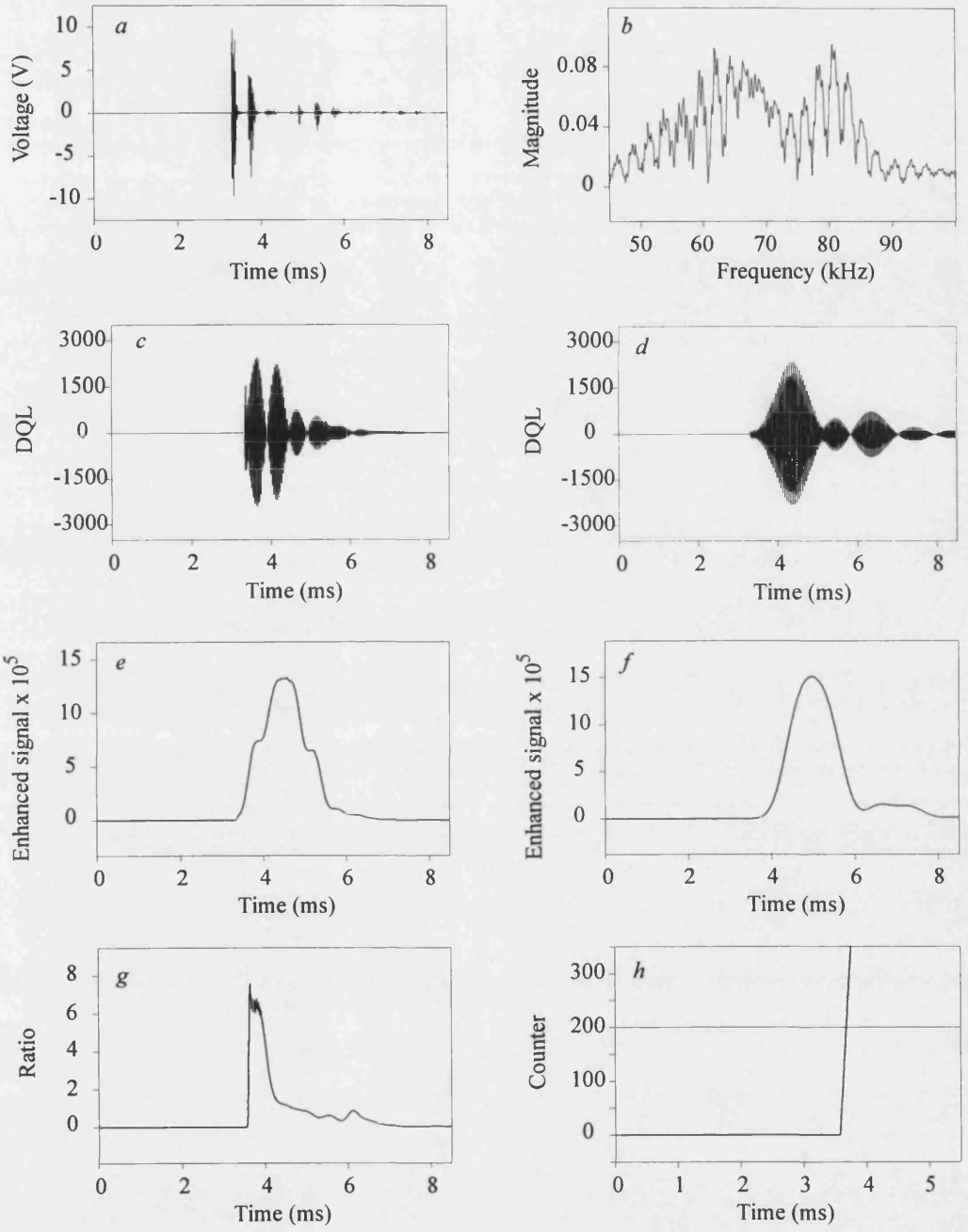
g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 6.48 Midpoint series compensation mode 2 relay response at end S



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

g Discrimination ratio

h Trip counter output

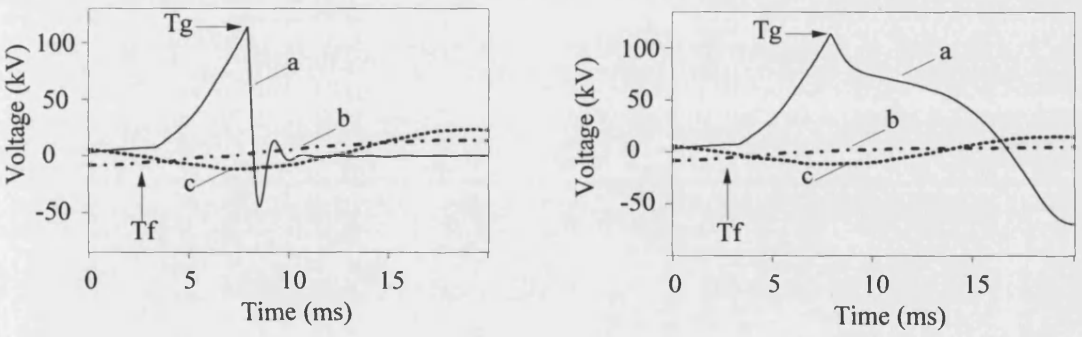
Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 6.49 Midpoint series compensation mode 2 relay response at end R

Figures 7.2 and 7.3; the relay asserts a trip decision in approximately 0.7 ms after fault inception.

Figure 7.4 shows the primary capacitor voltage waveforms at end R for the same fault condition. Here, the 'a' phase capacitor gaps flashover in approximately 5.5 ms after fault for both DGS and DGNS. The relay performance at End R for this particular fault condition is shown in Figures 7.5 and 7.6. Comparing the intermediate outputs with those at end S, it can be seen that there are some slight differences in the two cases.

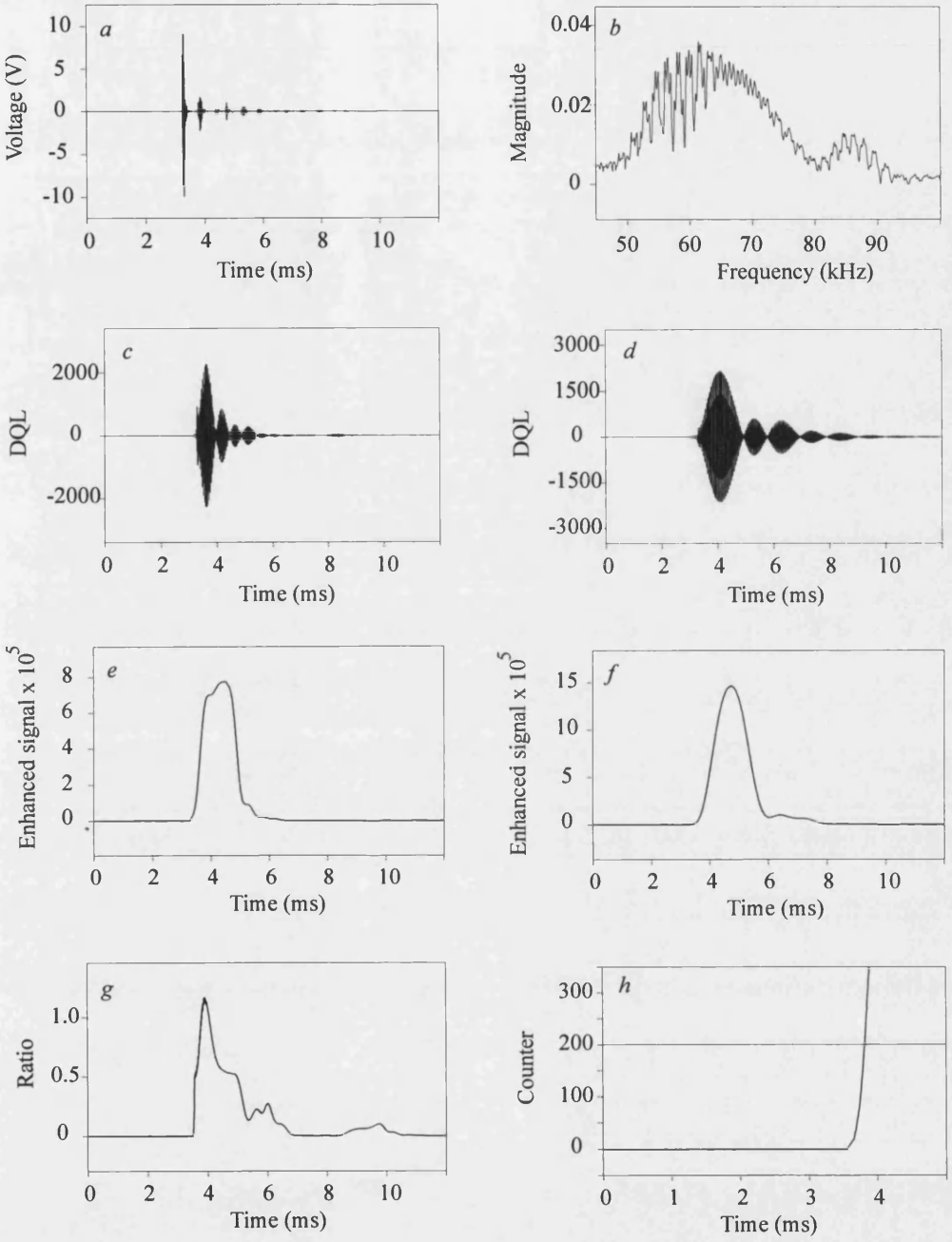


a With DGS
Fault inception, T_f = 2.5 ms

b With DGNS
Tg = capacitor-gap flash over

Figure 7.4 Capacitor voltage waveforms at end R for an internal fault

As expected the reduction in the signal magnitudes at End R is caused by the attenuation associated with the longer line (Figures 7.5a, 7.6a). The signals arrive at end R with an additional delay as they have a further distance to travel from the fault point. However, the relay response is very similar in both cases ie. systems employing DGS and DGNS, as shown in Figures 7.5 and 7.6; the relay asserts a trip decision in approximately 1.3 ms after fault inception.



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

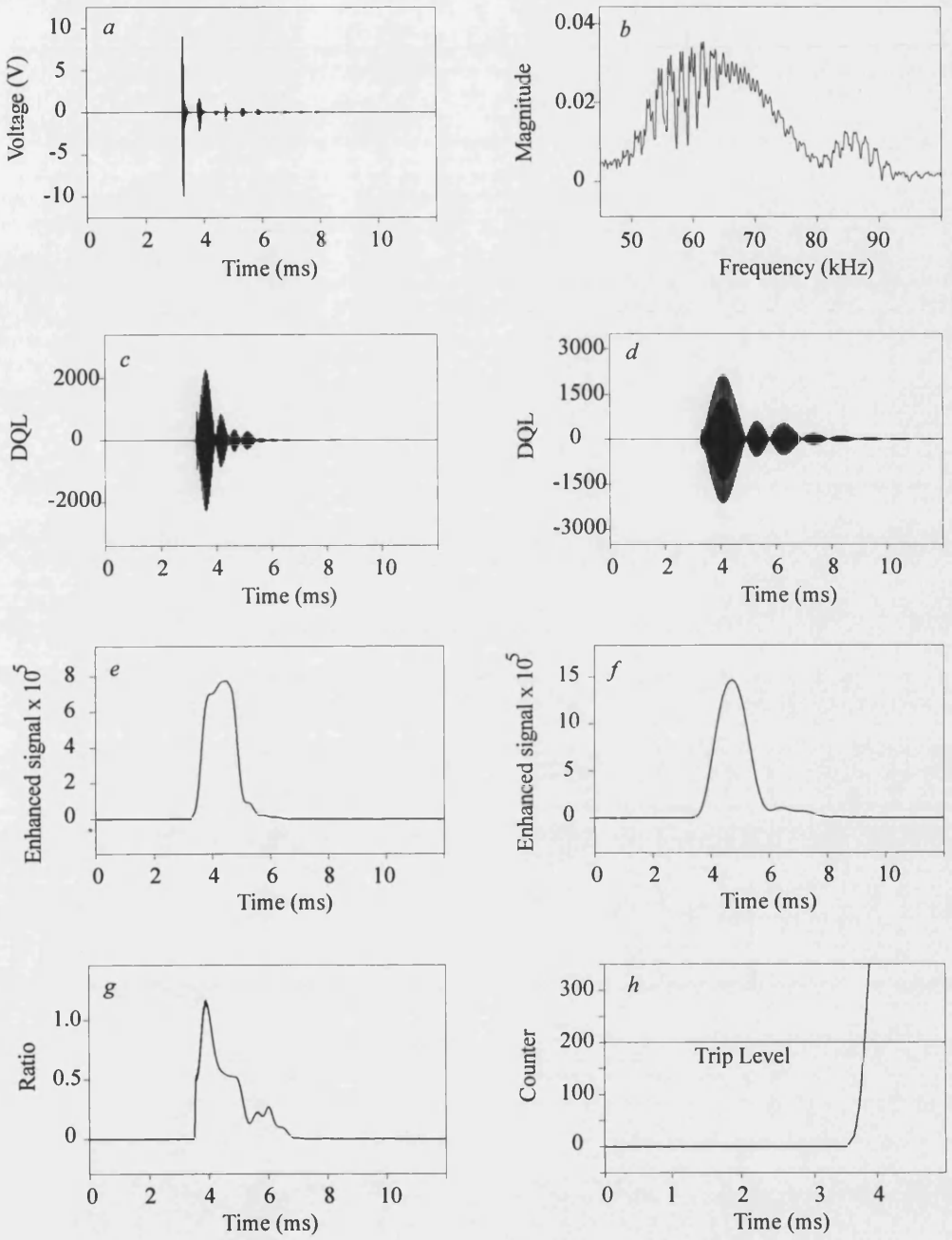
g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 7.5 Mode 2 relay response at end R for an internal fault with DGS



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

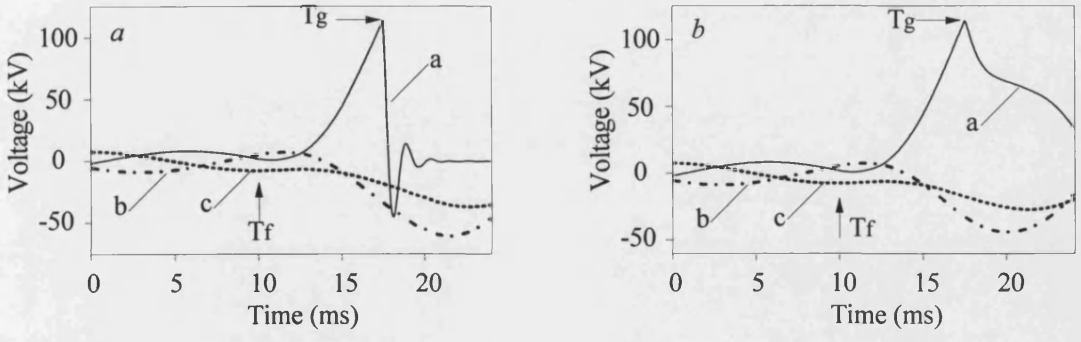
Figure 7.6 Mode 2 relay response at end R for an internal fault with DGNS

7.3 Typical External Fault Response

In series compensated systems, a potential problem exists in situations where a high level fault external to the protected line causes capacitor protection gap(s) to flashover; this in turn, causes a disturbance which can appear to be internal to the protected line. Therefore, it is important to verify that the relay performance is satisfactory under such situations.

An external 'a'-phase to earth fault is applied 10 ms after the start of the simulation very near to a voltage zero, immediately behind the line trap and on the busbar at the end S (at F_2 in Figure 4.2a); again both DGS and DGNS capacitor protective schemes are employed.

First of all, considering the primary system capacitor voltage waveforms at end S, Figure 7.7 shows that the 'a'-phase capacitor gaps at end S flashover in approximately 7.6ms after fault for both DGS and DGNS.



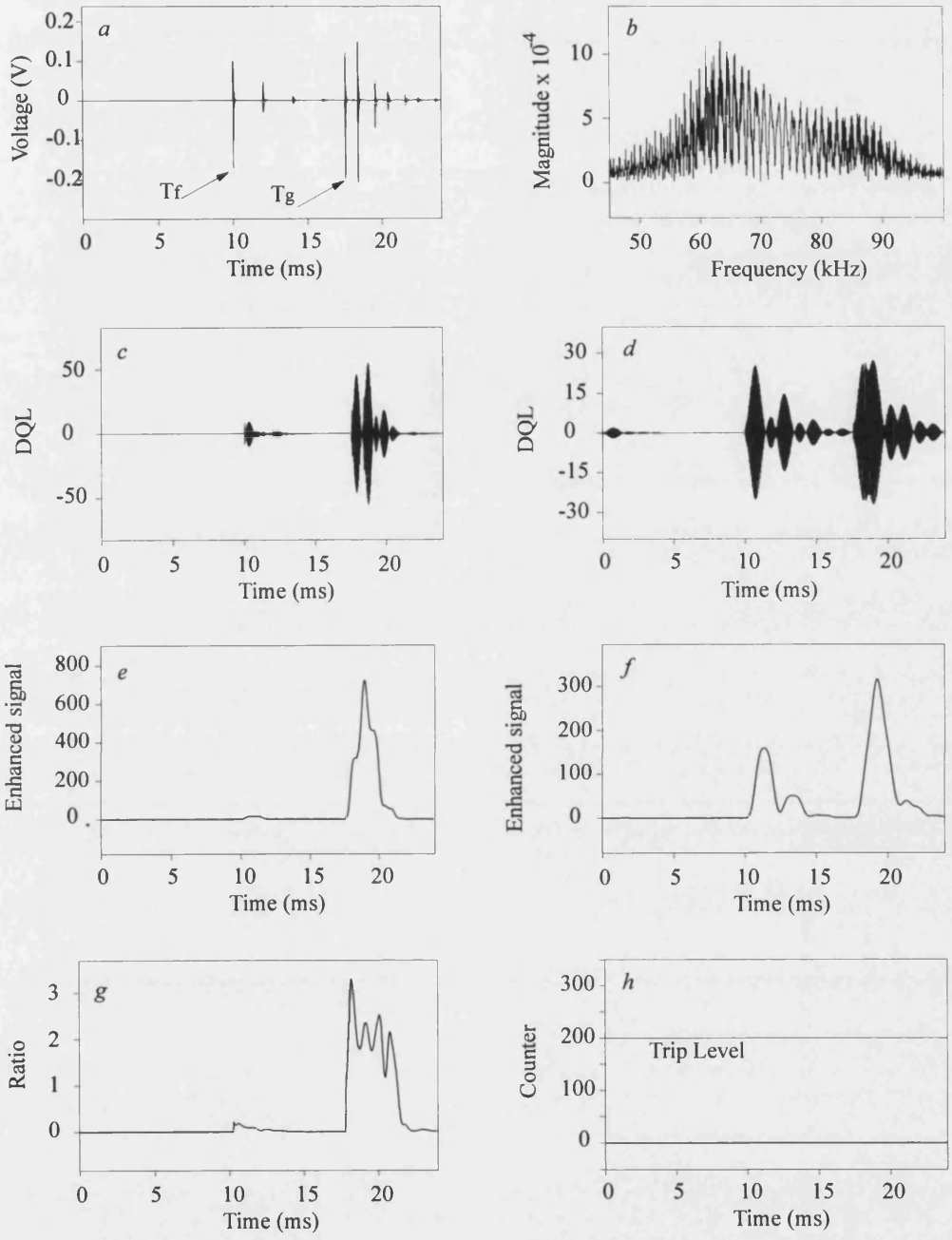
a With DGS
Fault inception, T_f = 10 ms

b With DGNS
Tg = capacitor-gap flash over

Figure 7.7 Capacitor voltage waveforms at end S for an external fault

The relay performance associated with aerial mode 2 (V_x) signal at end S was shown for both DGS and DGNS in Figures 7.8 and 7.9 respectively. Considering time domain response of the composite signal at end S, it is evident from Figures 7.8a and 7.9a that in the case of a DGS, the additional bursts of HF noise generated on gap flashover are much higher in magnitude than the corresponding bursts associated with a DGNS, and can be directly attributed to the relatively large voltage step change associated with the former on gap flashover. However, the net effect of this phenomenon is that the discrimination ratio in the case of the DGS rises above 'one' after gap flashover (ie. 7.5 ms after fault inception), but stays significantly below unity in the case of the DGNS. More importantly, the discrimination ratio stays well below unity for a significant time period after fault inception and as a consequence, the auxiliary scheme logic within the decision process (as described in chapter 5, section 5.3.4.2) recognises this as an external fault and inhibits any increment in the counter output once the pre-defined time window of 3 ms has been surpassed; this is evident from Figures 7.8h and 7.9h.

It is important to note that this potential problem due to gap flashover is only endemic in systems employing the relatively uncommon DGS capacitor protective schemes.



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

g Discrimination ratio

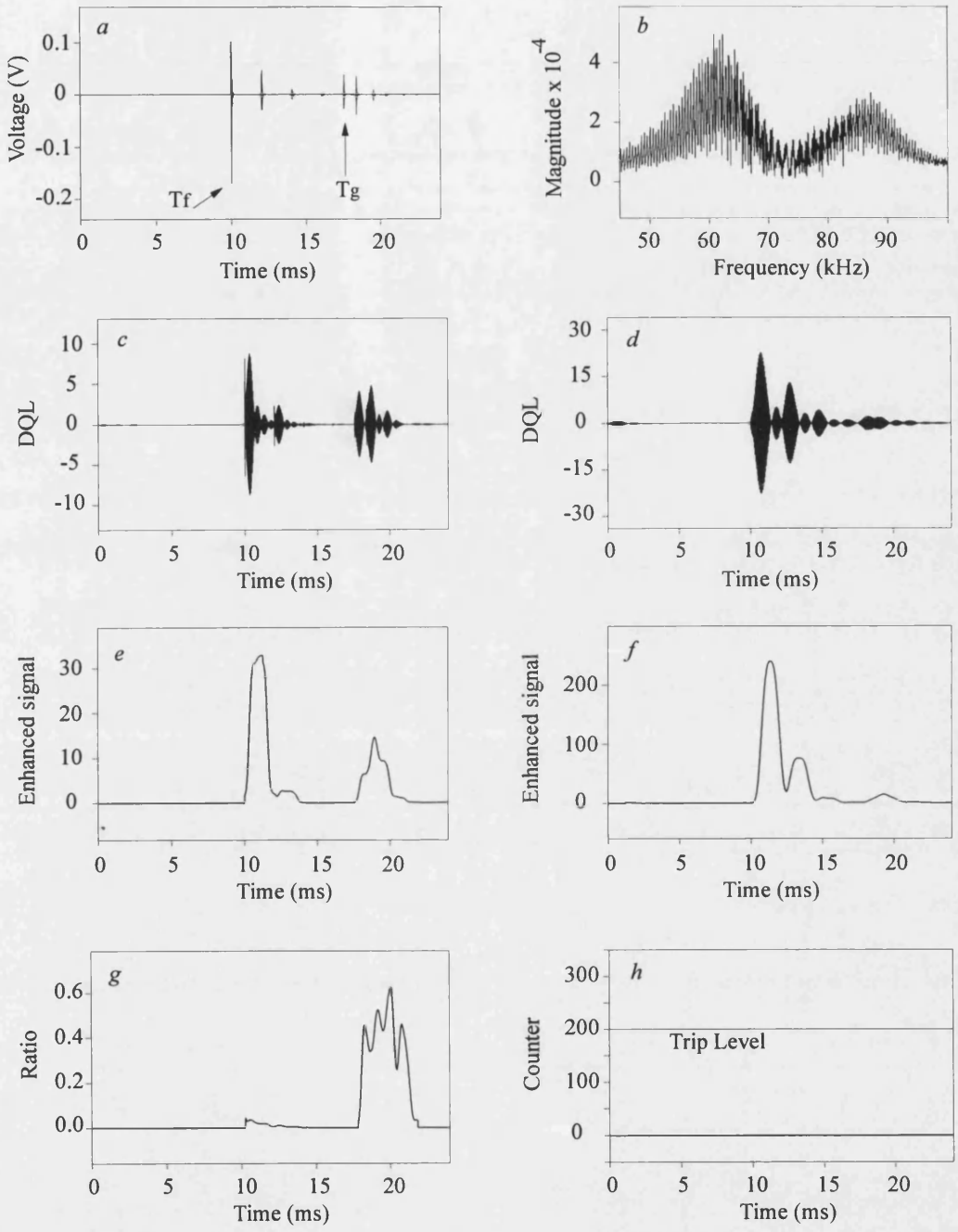
h Trip counter output

Fault inception, T_f = 10 ms

T_g = capacitor-gap flash over

DQL = Digital quantum levels

Figure 7.8 Mode 2 relay response at end S for an external fault with DGS



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

g Discrimination ratio

h Trip counter output

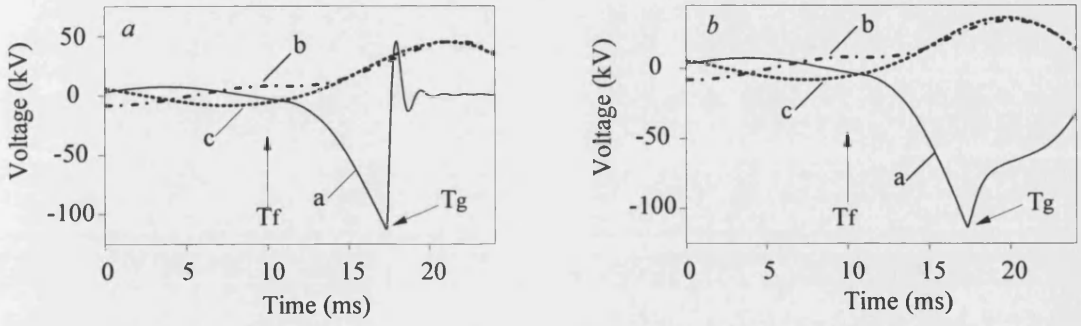
Fault inception, T_f = 10 ms

T_g = capacitor-gap flash over

DQL = Digital quantum levels

Figure 7.9 Mode 2 relay response at end S for an external fault with DGNS

The primary system capacitor voltage waveforms at end R for the same fault are shown in Figure 7.10; the mode 2 (V_x) relay response at end R is shown in Figures 7.11 and 7.12 for both DGS and DGNS respectively. In this particular fault study, the 'a'-phase capacitor gaps at end R flashover in approximately 7.4 ms after fault for both DGS and DGNS (Figures 7.10a and 7.10b). This clearly shows that the behaviour of the capacitor protective gaps differs significantly at the two line ends. This is somewhat as expected, because the equivalent impedances terminating each line end are different.

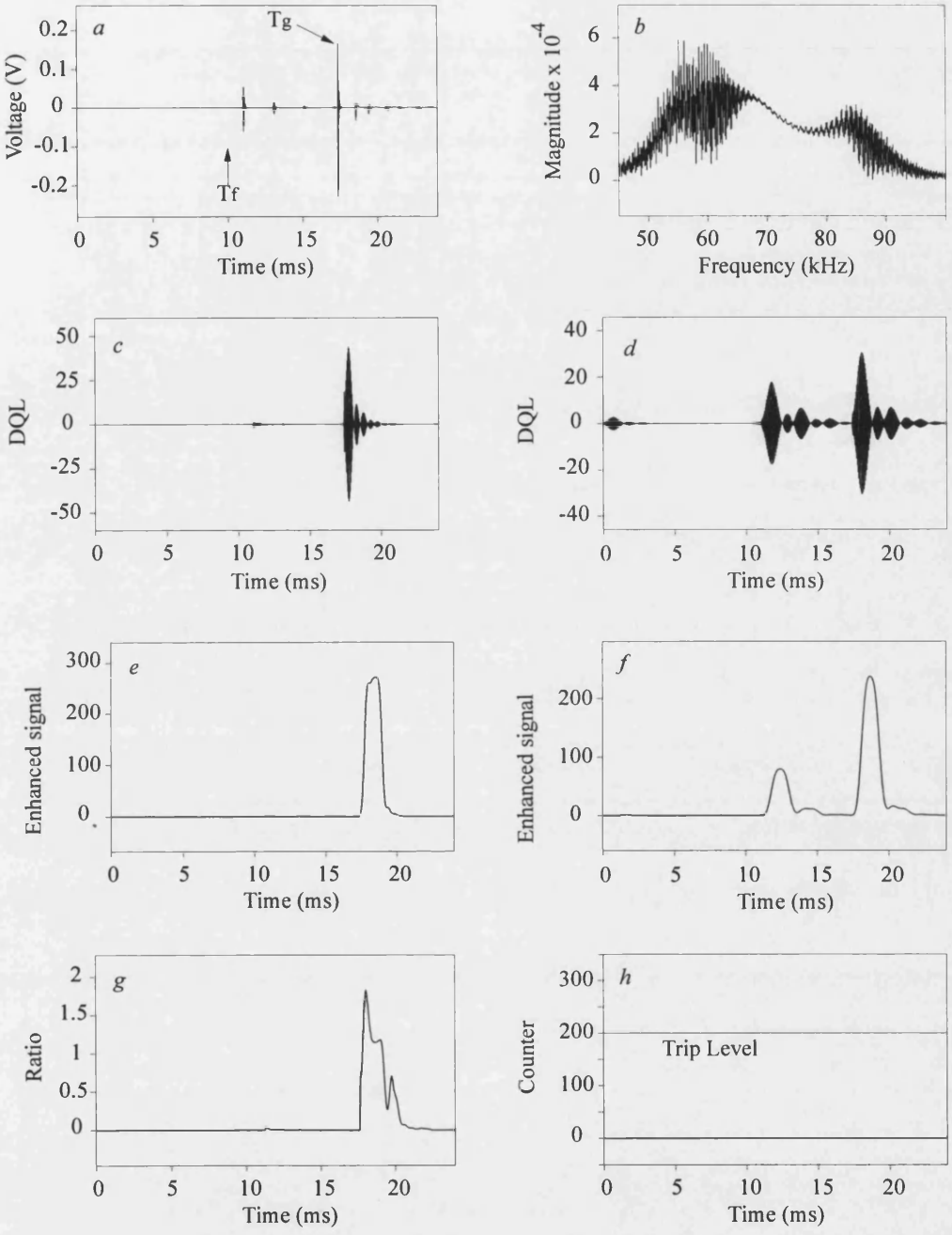


a With DGS
Fault inception, T_f = 10 ms

b With DGNS
Tg = capacitor-gap flash over

Figure 7.10 Capacitor voltage waveforms at end R for an external fault

As far as relay performance is concerned, the waveforms are essentially the same as those the end S and the magnitudes are reduced by the waves propagating through a longer line length and there is a corresponding increase in the travel time. However, here again in the case of DGS, the relative magnitudes of the additional HF noise generated on gap flashover is much higher than that associated with a DGNS and the discrimination ratio in the case of DGS once again rises above 'one' after gap flashover, while it stays significantly below unity in the case of the DGNS.



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

g Discrimination ratio

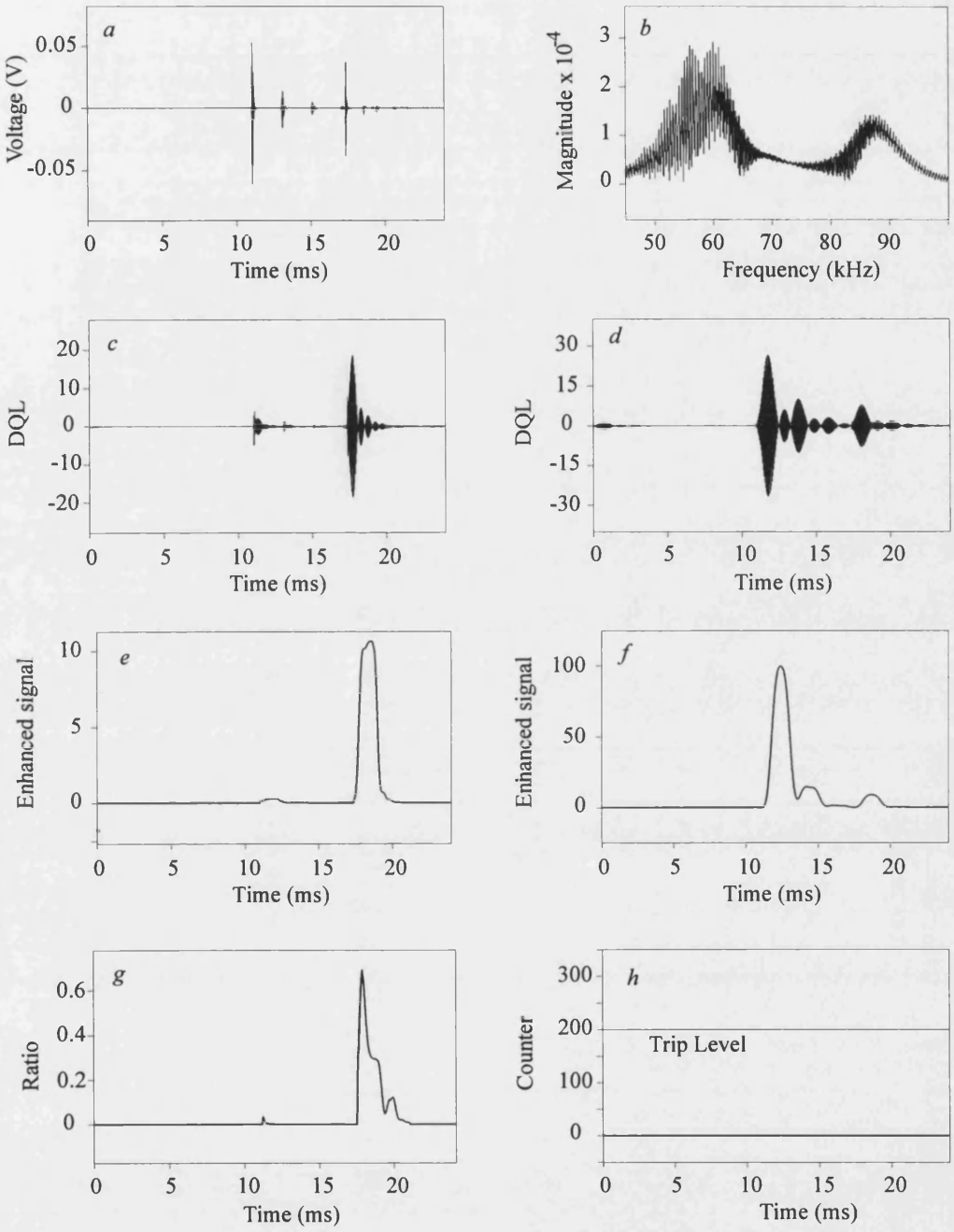
h Trip counter output

Fault inception, T_f = 10 ms

T_g = capacitor-gap flash over

DQL = Digital quantum levels

Figure 7.11 Mode 2 relay response at end R for an external fault with DGS



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

g Discrimination ratio

h Trip counter output

Fault inception, T_f = 10 ms

T_g = capacitor-gap flash over

DQL = Digital quantum levels

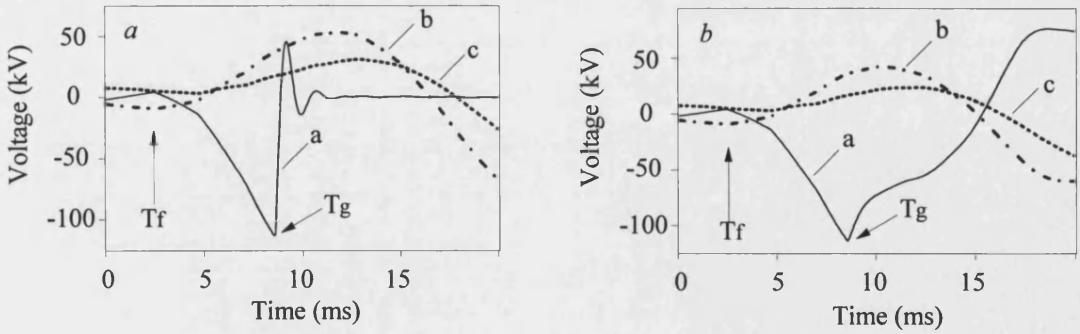
Figure 7.12 Mode 2 relay response at end R for an external fault with DGNS

However, the auxiliary scheme logic within the decision process recognises this as an external fault and inhibits the issue of a trip decision.

7.3.1 Effect of Fault Inception Angle on External Faults

An external 'a'-phase to earth fault near voltage zero at F_2 in Figure 4.2a has been discussed in some depth in section 7.3. The fault was applied just behind the line trap and on the busbar at end S and mode 2 (V_x) signals at both ends S and R have already been examined.

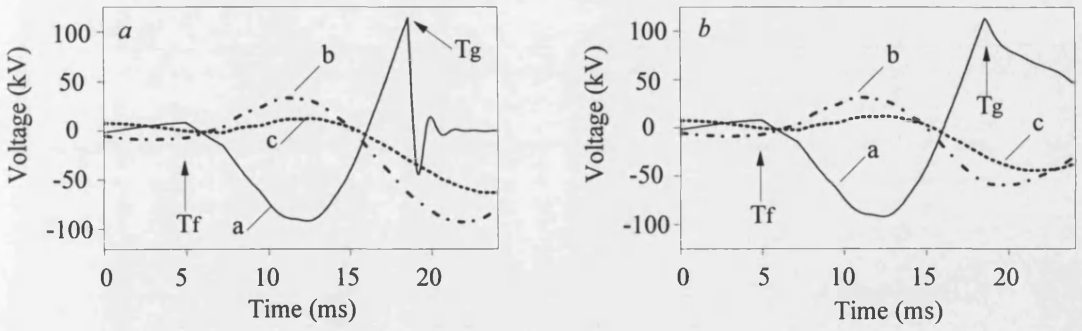
Increasing the fault inception angle to 45^0 and then 90^0 whilst keeping all the other parameters constant, has a significant effect on the signals generated. First of all considering the primary capacitor voltage waveforms at end S, Figures 7.13 and 7.14 show that the behaviour of the capacitor protective gaps differs significantly as the fault inception angle increases.



a With DGS
Fault inception, T_f = 2.5 ms

b With DGNS
Tg = capacitor-gap flash over

Figure 7.13 Capacitor voltage waveforms at end S for an external fault at 45^0



a With DGS
Fault inception, T_f = 5 ms

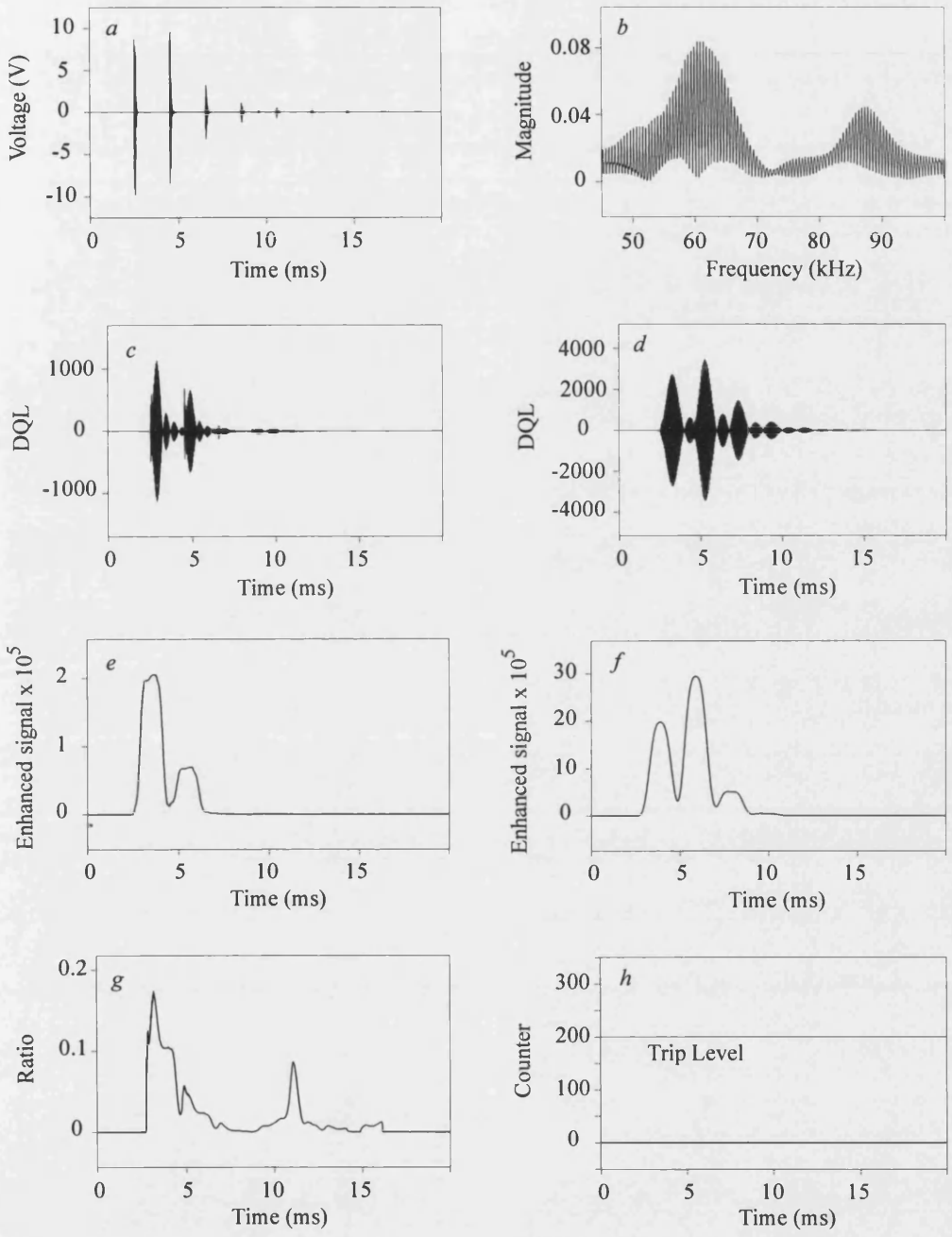
b With DGNS
Tg = capacitor-gap flash over

Figure 7.14 Capacitor voltage waveforms at end S for an external fault near voltage maximum

When the fault inception angle is 45^0, the 'a'-phase capacitor gaps at end S flashover in approximately 6.1ms after fault for both DGS and DGNS (Figures 7.13a and 7.13b). On the other hand, both DGS and DGNS capacitor gaps at end S flashover in approximately 13.5 ms after fault in the case of the fault inception angle of 90^0, as shown in Figure 7.14.

Here, the results show that there is less of a tendency for the capacitor gaps to flash over for faults near voltage maximum than near voltage minimum, and that the flashover times associated with the latter are generally lower. This is primarily due to the offset nature of the currents associated with voltage minimum faults, which in turn tend to offset the voltages across the capacitor banks to a degree sufficient for the protective gaps to spark over.

Figures 7.15 - 7.18 show the relay performance associated with the aerial mode 2 signal at end S for both DGS and DGNS with different fault inception angle. In marked contrast to the previous case of the voltage zero fault, the bursts of the HF signals generated by a genuine arcing fault (augmented by a significant travelling wave component) are much larger in magnitude in comparison to the additional HF components generated on gap flashover. As expected, for these external faults, the discrimination ratios remain well below unity and as a consequence, the relays remain stable for both DGS and DGNS, as clearly evident from Figures 7.15 to 7.18.



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

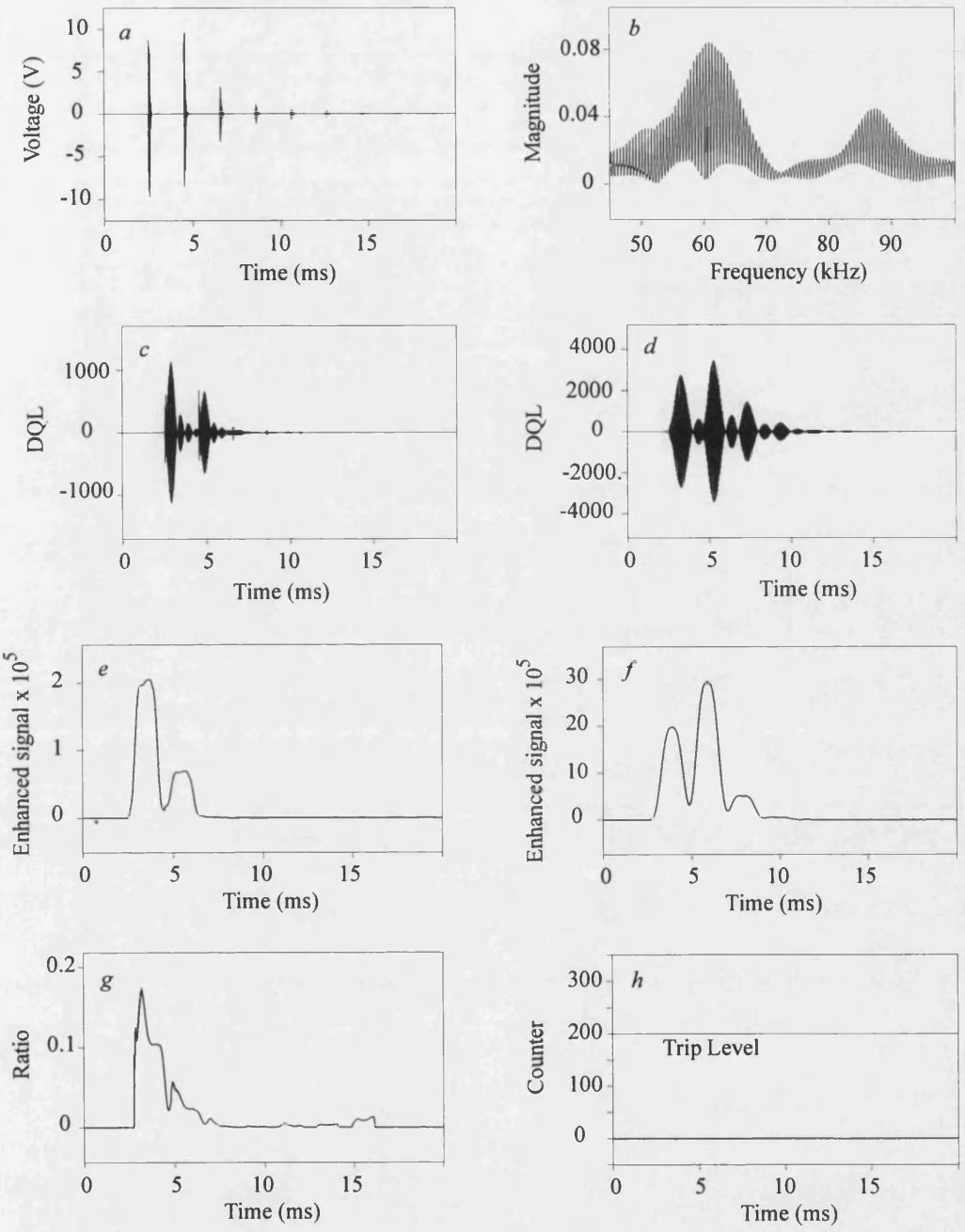
g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 7.15 Mode 2 relay response at end S for an external fault at 45^0 with DGS



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

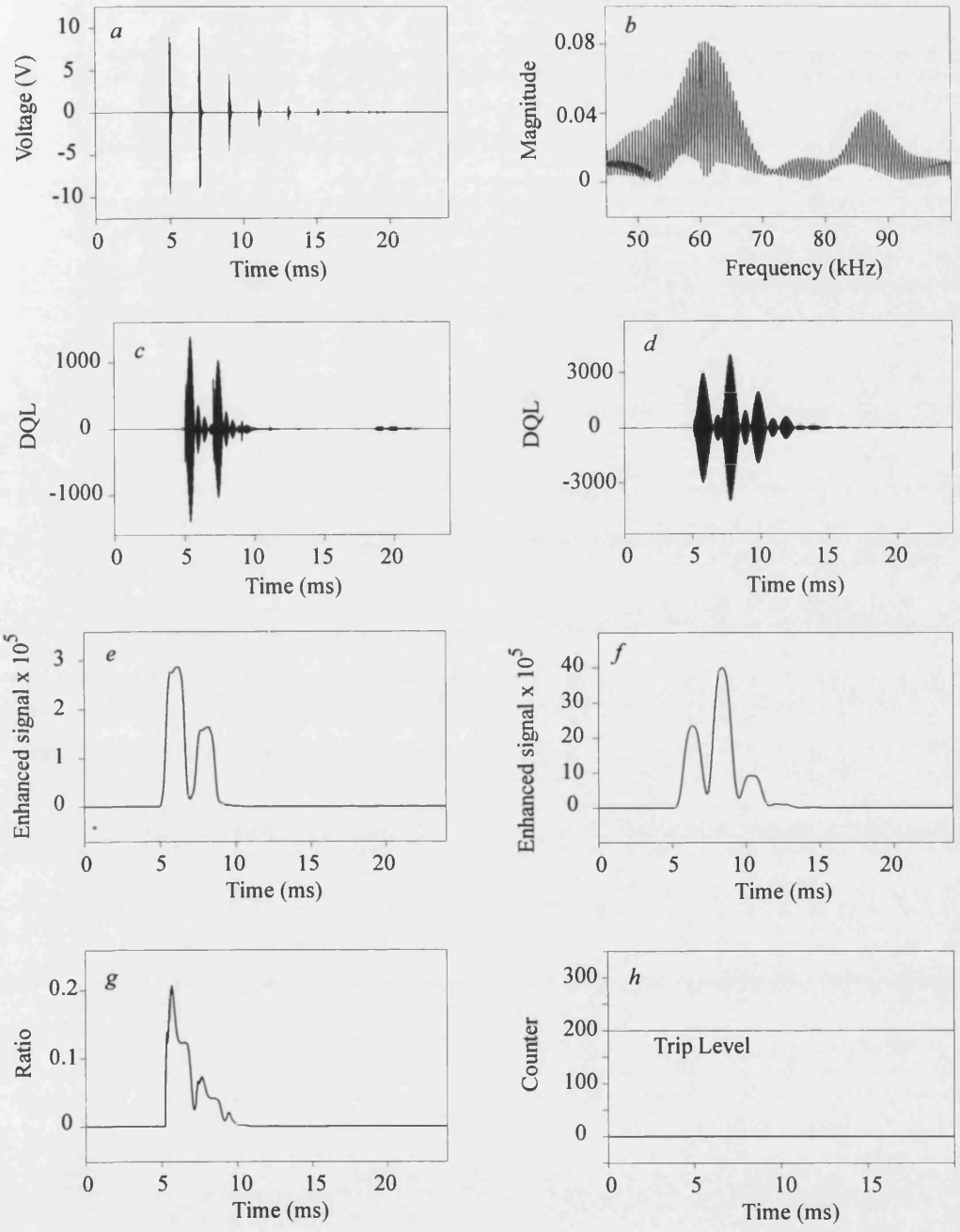
g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 7.16 Mode 2 relay response at end S for an external fault at 45^0 with DGNS



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

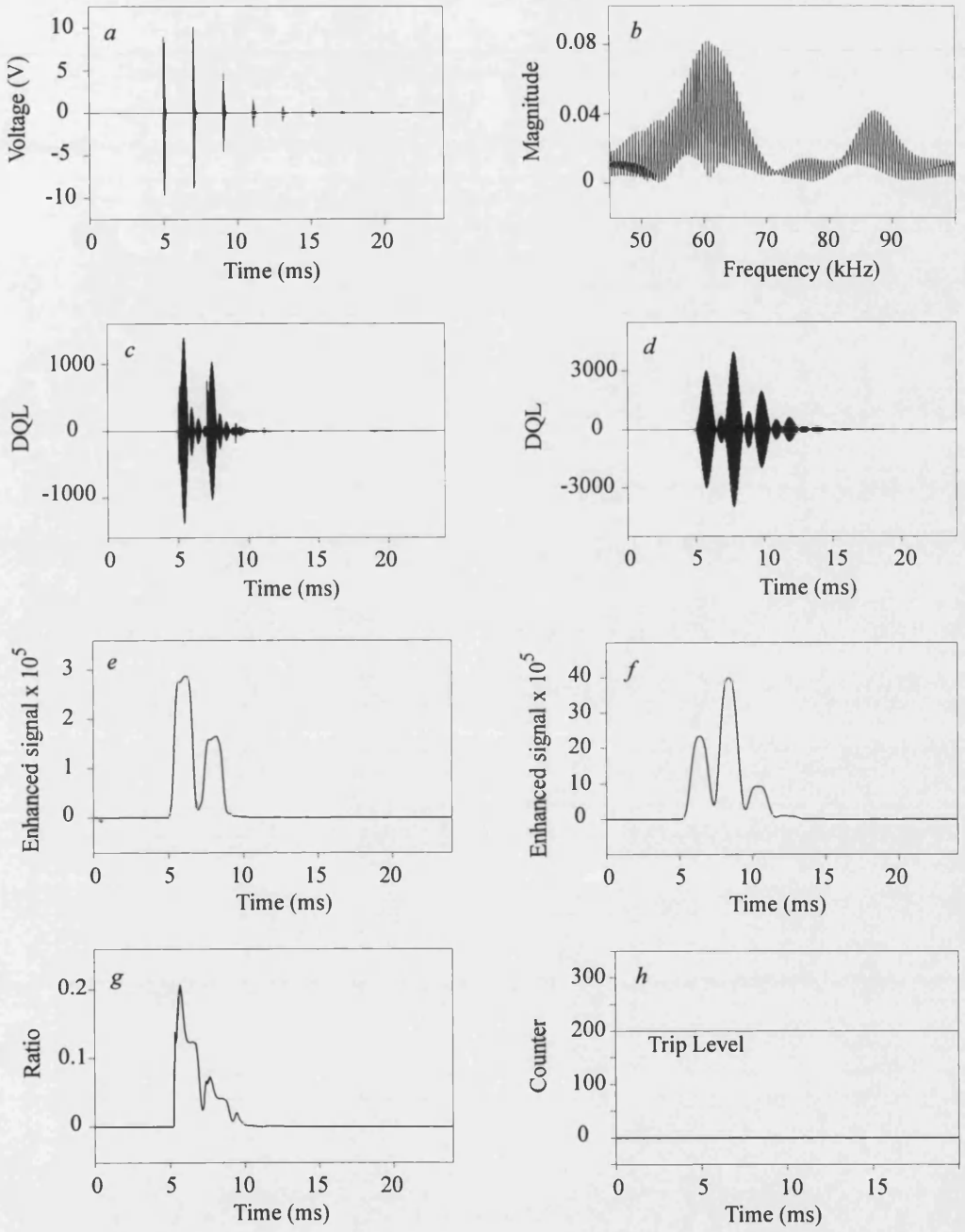
g Discrimination ratio

h Trip counter output

Fault inception, T_f = 5 ms

DQL = Digital quantum levels

Figure 7.17 Mode 2 relay response at end S for an external fault near voltage maximum with DGS



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

g Discrimination ratio

h Trip counter output

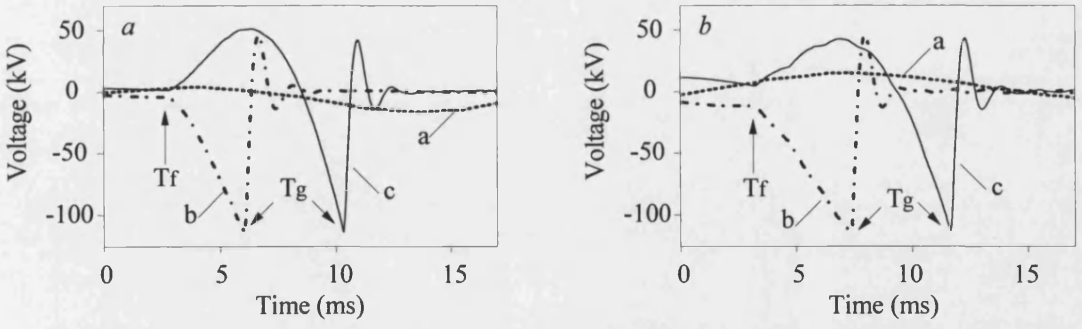
Fault inception, T_f = 5 ms

DQL = Digital quantum levels

Figure 7.18 Mode 2 relay response at end S for an external fault near voltage maximum with DGNS

7.4 Relay Performance for Other Types of Fault

Figure 7.19 shows typical capacitor voltage waveforms at each end of protected line following a 'b'-'c'-phase-earth fault at point F_{13} on the multi-section compensation feeder system of Figure 4.2d, when a DGS capacitor protective scheme is employed. The fault occurs when the 'a' phase voltage is going through 30^0. This particular fault condition results in phases 'b' and 'c' capacitor gap flashover, at end S in approximately 3.6 ms and 7.8 ms after fault (Figure 7.19a) and at end R in approximately 4.9 ms and 9.2 ms after fault (Figure 7.19b), respectively. It is thus apparent that for double-phase-earth faults, there can be appreciable stagger in the capacitor gap flashover times of the two faulted phase capacitors at any one end. Moreover, as expected, the behaviour of the capacitor protective gaps differs significantly at two line ends. This is again due to the source side networks and the equivalent impedances terminating each line end being different.



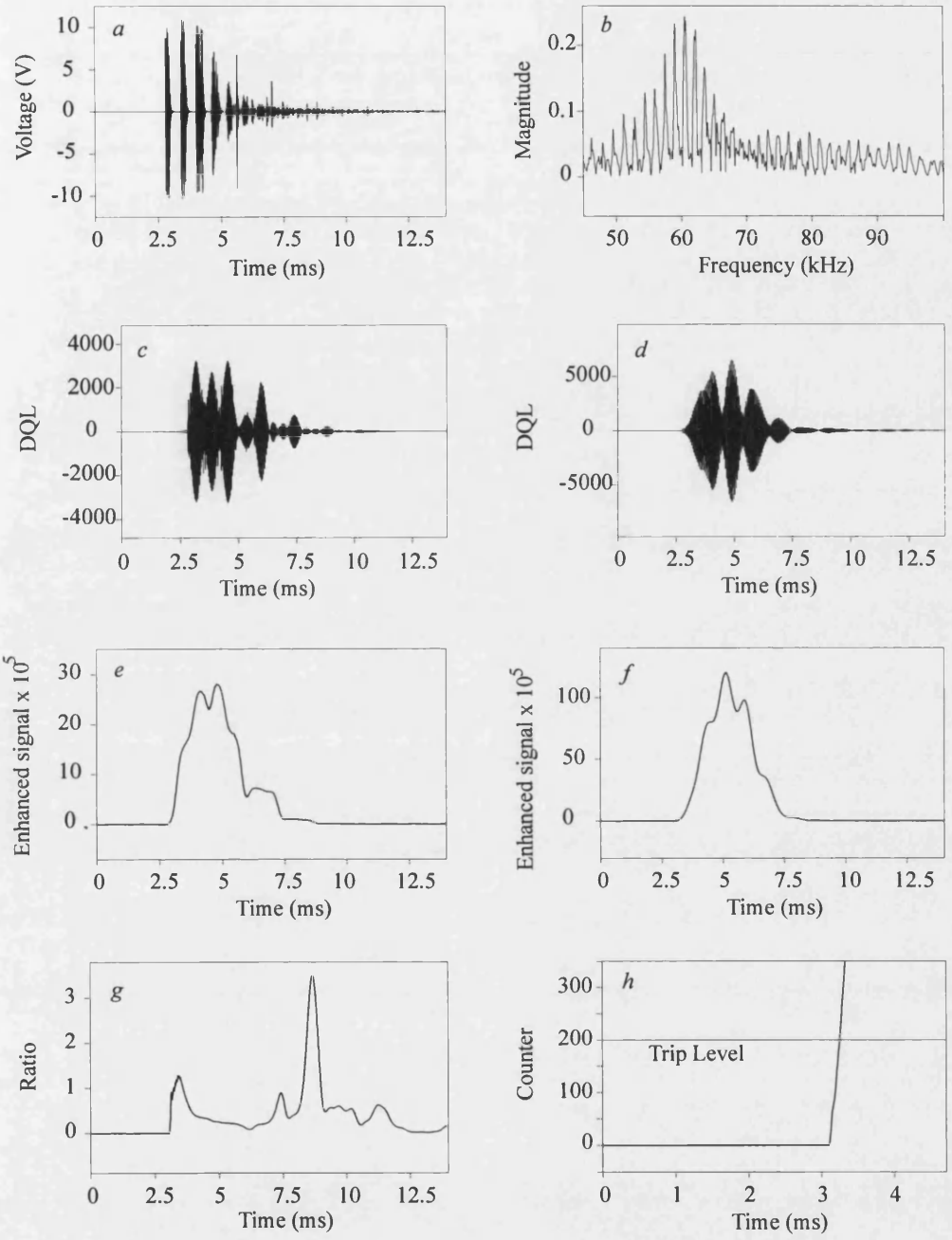
a End S
Fault inception, T_f = 2.5 ms

b End R
Tg = capacitor-gap flash over

Figure 7.19 Capacitor voltage waveforms for a B-C-E fault with DGS

Figure 7.20-7.21 show the mode 2 (V_x) outputs at the both ends for this particular fault. As this is a phase to phase earth fault, HF signals of large magnitudes are generated. Consequently, the signals captured by the stack tuners have to be clipped. The magnitudes of the signals received at each end are determined by the distance between the fault and the measurement equipment. The end R signals are attenuated the most, as they travel the furthest distance. This can be clearly seen by comparing the filter outputs at the two line ends (Figure 7.20c,d, 7.21c,d). The discrimination ratios at both line ends exceed unity and the relay asserts a trip decision at ends S and R in approximately 0.76 ms and 1.08 ms after fault inception, respectively.

Although not shown here, there are also small variations in the gap flashover times for both phase to phase faults and three phase to earth faults; more importantly, the relay performance is satisfactory for both internal and external faults under such conditions.



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

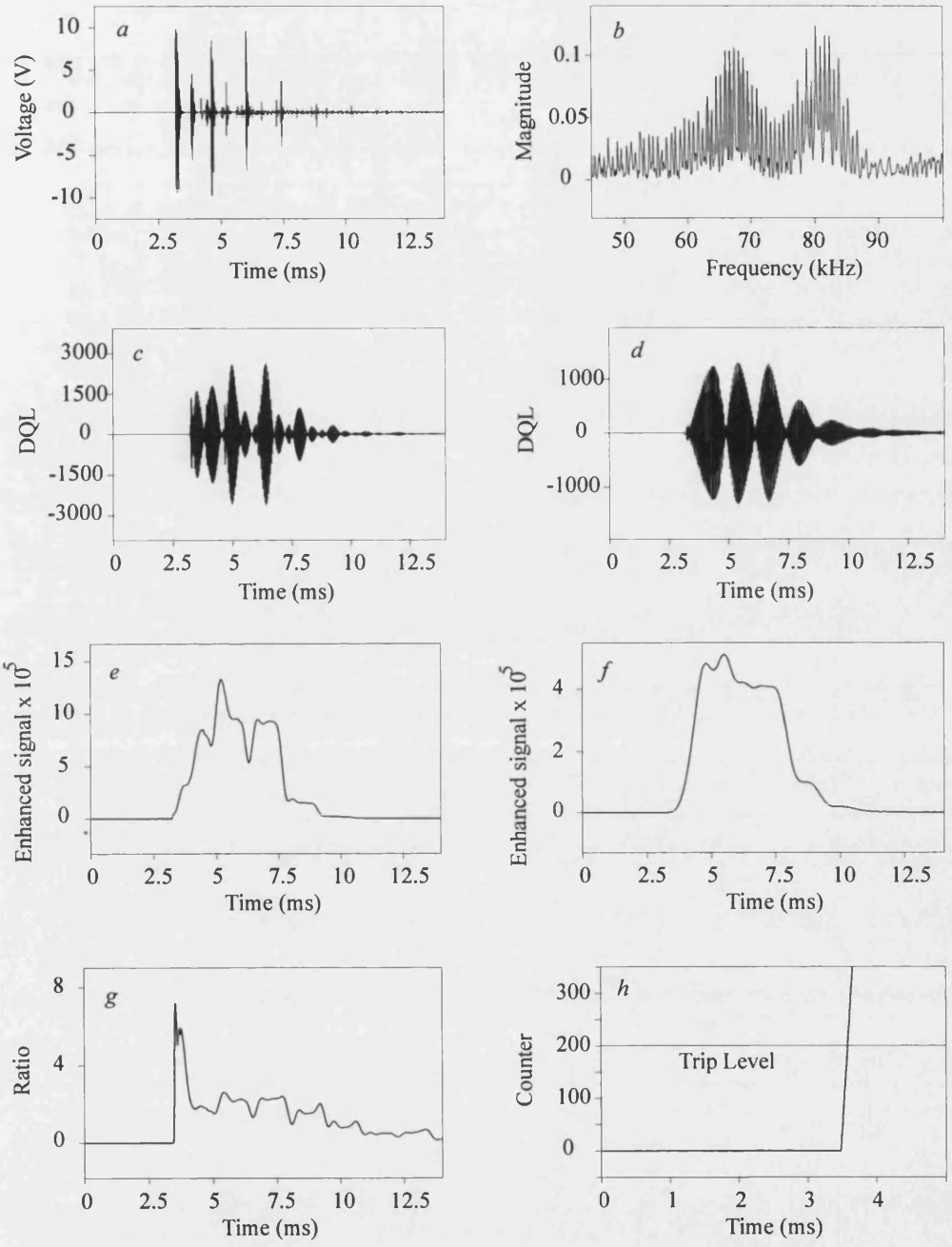
g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 7.20 Mode 2 relay response at end S for a B-C-E fault with DGS



a Analogue modal signal

b Frequency spectrum of *a*

c Operate filter output

d Restraint filter output

e Enhanced operate filter ouput

f Enhanced restraint filter output

g Discrimination ratio

h Trip counter output

Fault inception, T_f = 2.5 ms

DQL = Digital quantum levels

Figure 7.21 Mode 2 relay response at end R for a B-C-E fault with DGS

7.5 Overall Relay Performance

Like the cases for the MOV capacitor protective scheme, a series of different types of faults were simulated at various points on the protected line for the arrangements shown in Figures 4.2a-d with conventional DGS and DGNS schemes. The faults again cover a wide selection of fault positions, inception angles and types; the results are summarised in Table 7.1; here again, the results clearly show that the relay performance is satisfactory.

Table 7.1 Overall relay performance with trip times

Note: Fault angle is the angle of 'a'-phase voltage at end S

Fault characteristics, capacitor location and type of capacitor protective scheme E - Line end compensation M - Midpoint compensation				Time to trip after fault inception (ms) N/OP - No Operation			
				Line end S relay		Line end R relay	
Position	Angle	Type	Details	Mode V_x	Mode V_y	Mode V_x	Mode V_y
F_5	-30^0	B-C	70% E DGS	0.40	0.39	1.39	1.39
F_8	10^0	A-B-E	70% E DGNS	N/OP	N/OP	N/OP	N/OP
F_{10}	45^0	A-E	50% M DGNS	0.62	0.62	1.18	1.28
F_{12}	90^0	A-B-C	50% M DGS	N/OP	N/OP	N/OP	N/OP
F_{13}	30^0	B-C-E	70% E DGS	0.76	0.76	1.08	1.11
F_{14}	-120^0	C-E	70% E DGNS	N/OP	N/OP	N/OP	N/OP
F_{15}	-45^0	A-B	70% E DGS	N/OP	N/OP	N/OP	N/OP

CHAPTER 8

CONCLUSIONS AND FURTHER WORK

8.1 Summary of Work

This thesis presents a novel protection technique for accurately detecting faults on series compensated EHV transmission line using fault generated HF voltage signals. Although the fundamental principles are an extension of those reported in [34, 35] for plain feeders, they have been significantly modified to cater for the more complex series compensated transmission system. The work presented in this thesis thus outlines the progress made in the further design, development and application of the aforementioned principles to series compensated lines. Particular emphasis has been placed to evolving a design that overcomes the longstanding protection problems associated with series compensated lines. In this respect, it is vitally important that the system simulation be as accurate as possible within the bounds of practicality. Therefore, the system simulation of the power system has been carried out using the

EMTP software including detailed modelling of transmission systems, the capacitor bank, and the various types of independent capacitor protection equipment; this is essential to properly and comprehensively test the protection algorithm and strategies. Great attention is focused upon the modelling of the modern MOV capacitor protection units.

The fault generated HF voltage signals are captured with specially designed stack tuner circuits which are connected to each phase via the coupling capacitor of standard capacitor voltage transformers. The phase signals are first stepped down by an auxiliary transformer and are then combined to form two aerial modal signals which are fed into a signal processing unit. The modal transformation method is employed in the application to decouple the phase signals into their respective modes. This removes the common mode which minimises any mutual coupling effects. Two digital narrow bandpass filters are used to extract the necessary information from these modal signals. The outputs of the bandpass filters are enhanced to give a measure of spectral power and are then compared to give a discrimination ratio. This discrimination ratio is used to activate a sophisticated decision process which is used to determine whether a fault is internal or external to the protected zone.

The relay performance has been demonstrated by simulating a variety of internal and external faults on different 500 kV series compensated networks employing different types of capacitor protective schemes. In particular, attention is give to the modelling of the non-linear MOV elements. The simulations contain a primary arc model which takes into account the time varying behaviour of the electric arc. All system

simulations are carried out using the universally accepted EMTP software and single circuit 500 kV transmission line have been modelled with frequency dependent parameters.

8.2 General Conclusions

The results presented clearly show that the new relay scheme is able to overcome many difficult protection problems encountered on series compensated lines using conventional methods, and discriminates clearly between internal and external faults, producing a fast trip output. The new relay technique is inherently tolerant to fault position, fault inception angle, fault type and resistance within the fault path. In addition, the scheme is insensitive to differing system conditions such as variations in busbar capacitance, and source side network configurations and it is immune to any problems caused by the line loading. This can be directly attributed to the line trap and busbar shunt capacitance forming a strong barrier between the circuit being protected and the rest of the power system. These qualities of the relay can be directly attributed to the fact that the relay principle is largely independent of the actual magnitudes of the HF signals and is totally dependent on utilising the characteristic features of the fault generated HF signals, the latter being uniquely retained for different system and fault conditions encountered in practice. Furthermore, although for certain types of faults, the signal levels have to be clipped in order to accommodate a dynamic range covering a large variety of practically encountered faults, the relay performance is not unduly affected as a result of loss of signal power.

The relay algorithm developed, including the special decision process, enables the scheme to give correct performance under all types of practically encountered faults. Also the results presented clearly show that the relay maintains its dependability and security for systems employing different types of capacitor protective schemes and is virtually immune to changes in compensation/additional transients emanating from the operation of such schemes under faults. This is a significant advantage over conventional line protection relays.

Furthermore, a sensitivity analysis has established that the designed relay is stable for external faults and gives correct trip outputs for internal faults when there are small parameter variations, for example, in the line traps and/or stack tuners, that might occur in practice. This clearly demonstrates the robustness of the relay and can be largely attributed to the digital filter and the sophisticated decision logic designs.

This new protective technique based on non-unit principle, signifies an important breakthrough in the protection of series compensated lines which, although highly attractive both from an economic and environmental points of view, hitherto have found limited applications in view of less than satisfactory performance being possible with conventional non-unit protection techniques. It should be mentioned that although the technique described herein is designed for transmission systems employing power line carrier equipment comprising specialized line trap/stack tuner units and can therefore involve additional costs, the alternative for satisfactory protection of series compensated lines would be unit-type protection based on expensive communication links.

Simulation results have also shown that correct trip decisions can be made in approximately one millisecond after fault inception for all the different system and fault conditions studied. The simulation and subsequent calculations are performed off-line and so do not take into account any delay due to the analogue processing or the time taken for the processors to perform the necessary calculations. It is envisaged that a hardware implementation of this relay would use high performance floating point parallel processors. The overall tripping time of the protection relay using these processors would still be under about five milliseconds.

8.3 Suggestion for Further Work

As emphasised in the thesis, the protection scheme has been designed using CAD techniques including emulation of analogue interface and hardware. This effectively means that the relay performance depicted is close to what might be expected in practice. However, as a next logical step, the prototype protection relay should be built and tested in real time. In this respect, it is very important to ensure that the protection relay algorithm is executed on the prototype hardware in real time (ie. well within the microprocessor duty cycle) at the required sampling rate of 200 kHz. In this respect, some preliminary studies have indicated that four Texas Instruments TMS320C40 parallel processors would be able to perform all of the necessary calculations within the 5 μs (ie. sampling rate of 200 kHz) sampling interval. The prototype hardware could then be tested in real time using both simulated data and practical data using a programable transmission line (PTL) test facility.

The simulated data would enable the prototype to be tested for a very large number of fault conditions and situations that may be encountered in practice, for example, different types of capacitor protective schemes and different values of degree of series compensation etc. In practice there is always a level of spurious noise present on the measured signals and this can have some bearing on the performance of the relay. The practical data has the advantages that it is from a real situation and so would include some typical spurious noise levels impressed upon the signals.

The final testing procedure would involve testing the prototype relay under service conditions. This would mean installing the prototype relay at a substation and supplying it directly from the stack tuner output in a field trial. This is, of course, the most comprehensive test environment but it is very expensive and has a number of potential problems. Initially it relies on finding a suitable complete test circuit (ie. a 500 kV series compensation system with 3-line trap/stack tuners) with an electricity transmission company which is willing to co-operate. In this case, the existing PLC equipment would have to be modified in the way of installing a third phase line trap and stack tuner at each end of the circuit; it should be noted that in systems employing conventional PLC equipments, it is normal practise to install the line traps on only two of the three phases.

With the advent of FACTS devices, it is important to test the new protection relay on systems employing variable compensation which by nature can introduce HF transients due to the presence of thyristors, etc. Moreover, although not very common, there are also around, composite circuits comprising overhead lines and

small sections of underground cables; since the latter have significantly different characteristics to the former, the transients introduced under faults on composite circuits can be quite different from those introduced on circuits comprising purely of overhead lines; it is thus also important to evaluate the relay performance for such circuits.

The work done sofar has been confined to relay design and testing on single circuit systems only for different system conditions. Although double circuit series compensated transmission systems are relatively uncommon, the relay must also be tested for a double circuit system, where there is another infeed route to the fault point.

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APPENDIX A

SIMULATION OF THE MOV CAPACITOR PROTECTIVE SCHEME

The capacitor protection must be accurately modelled in the protection scheme to accurately transfer the voltage across the capacitor. A typical circuit configuration of a MOV protected series capacitor is shown in Figure 4.7. A number of design parameters of series capacitor protective are important for the detailed simulation. A quantity which is frequently used is termed the protective level current I_{pr}. This current determines the protective level voltage and is specified as a multiple (typically 2.0 to 2.5) of the rated capacitor bank current or full load current, I_{fl}.

If the volt ampere characteristic of a particular MOV-based protection is known, an elaborate multi-exponential zinc oxide model is available within the EMTP software to accurately reproduce this data. However,when the specific characteristic is not available, the nonlinear volt ampere characteristics of an MOV can be approximated

in analytical form by the familiar single exponential model:

$$I = \left[\frac{V}{V_N}\right]^n \qquad \text{(A-1)}$$

where V_N is a characteristic voltage of the arrestor which defines the proportionality between I and V^n. The value of n is typically chosen from 30 to 50. To determine V_N, I_{max} (peak) is substituted for I and V_{pk} for V. I_{max} is the current that causes the triggered air gap to flash and if it is unknown, an assumed value of 15-20 kA can be used. V_{pk} is the peak protective voltage level of MOV and can be calculated as:

$$V_{pk} = \sqrt{2} I_{pr} X_c \qquad \text{(A-2)}$$

where X_c is the reactance of the capacitor bank and I_{pr} is the protective current level of MOV as described above. The MOV is designed to operate randomly according to different fault conditions and to hold the capacitor voltage at or below the value of V_{pk} even for the largest available system current I_{max}.

In the studies presented herein, a typical line loading of 500 kV line of 1 GVA is assumed and the characteristics of the MOV are obtained as follows and summarised in Table A.1.

Full load current, I_{fl} $= 1000 \times 10^3 / (\sqrt{3} \times 500)$

$= 1.1547$ kA

Protective current level of MOV $= 2.5 \times 1.1547$

$= 2.8868$ kA

Peak protective voltage level of MOV, $V_{pk} = \sqrt{2} \times 2.8868 \times 31.881$

$= \underline{130.15 \text{ kV (peak)}}$

Note : for 70% compensation capacitor reactance X_c = 31.88 from Table 4.2.

Assuming that n= 32 and I_{max} = 15 kA (peak) and substituting those values in Equation A.1:

$$15 \times 10^3 = \left[\frac{130.15 \times 10^3}{V_N}\right]^{32} \qquad \text{(A-3)}$$

$$\therefore \quad V_N = 96 \times 10^3$$

Therefore, for 70% compensation with capacitor banks at line ends, the MOV characteristic is given by:

$$I = \left[\frac{V}{96 \times 10^3}\right]^{32} \qquad \text{(A-4)}$$

The MOV parameters for various levels of compensation are summarised in Table A.1.

Table A.1 MOV characteristics for different levels of compensation

Type of scheme	Level of compensation	MOV parameters	
		V_{pk} (peak) (kV)	V_N (kV)
Two capacitor banks	Total 70% (35% for each)	130.15	96
	Total 50% (25% for each)	92.96	69
	Total 30% (15% for each)	55.77	41
One capacitor bank	50%	185.96	138

PUBLISHED WORK

The following papers are based on the work described in this thesis. Copies of Papers 2 and 4 are enclosed for reference.

[1] R.K. Aggarwal, J.A.S.B. Jayasinghe, Z.Q. Bo, and A.T. Johns, " A new approach for discriminating between switching and fault generated broadband noise on series compensated EHV transmission lines", *International Conference on Advance in Power System Control, Operation & Management, APSCOM-95, Hong Kong Convention & Exhibition Center*, November 1995.

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A NEW APPROACH TO MEASURING FAULT GENERATED HIGH FREQUENCY NOISE ON SERIES COMPENSATED EHV TRANSMISSION LINES.

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ABSTRACT

EHV transmission lines employing series capacitors pose many protection problems for conventional protection techniques, not ordinarily encountered with plain feeders. However, there is evidence to suggest that the relatively new concept based on non-power frequency components can provide an attractive alternative. This paper describe a new technique for modelling and the measurement of fault generated high frequency signals associated with series compensated EHV line application.

1. INTRODUCTION

Benefits of installing series capacitors in the power system include increased power transfer capability, improved power system stability, reduced system losses, improved voltage regulation, and regulation of power flows[1]. There are, however, difficult problems encountered in the protection of such lines, and these arise primarily as a result of the rapid circuit parameter changes due to the operation of the capacitor protective equipment[2,3]. This in turn causes rapid changes in the measured effective system impedance and is therefore a serious impediment to the operation of impedance measuring devices, the majority of which are based on power frequency components. If the capacitor is protected by a non-linear metal-oxide varistor (MOV) element, the capacitor compensation is a function of the fault location. Thus, due to the varying amount of capacitance in the circuit, distance relays may misoperate and fault locators may not be able to accurately determine the fault location.

Furthermore, the non-linear nature and the random behaviour of the capacitor protective gap characteristics, in particular those associated with non-linear resistor-type schemes, inevitably results in the generation of high frequency (HF) noise, in addition to the fault generated HF noise. The former, although of no consequence to power frequency based protective relays, can nevertheless pose problems for the protective relay techniques based on non-power frequency components.

High frequency signals generated on EHV lines caused by the sudden change in the system voltage that occurs in the immediate post-fault period, due for example to arcing faults, are generally outside the bandwidth of receptibility of most conventional capacitor voltage transducers(CVTs). However, it has been recently suggested[4] that these signals could be used very effectively to develop new types of protection schemes that would have many advantages over existing power frequency measurement based methods; there are fast decision making, immunity to power swings and heavy loading, insensitivity to fault path resistance, etc. However, before a HF-based protective relay for series compensated lines can be effected it is extremely important to be able to accurately model the HF signals impressed upon the line under capacitor protective gap operation.

This paper describes a new technique for modelling and the detection of fault generated high frequency signals associated with typical 500 kV series compensated EHV line application. Particular attention is paid to the aforementioned protective gap generated noise problem and its effect on fault transient waveforms, and the responses are examined for a number of practically encountered different capacitor protection circuits and fault conditions. The paper then shows the effect of fault inception angle and fault position on the high frequency signals captured by specially designed stack tuners, via the high voltage capacitor of the CVT, in particular the effect on the frequency spectra of the HF signals for both internal and external faults are illustrated. In the research, the well known EMTP software is used for the simulation of series compensated EHV transmission systems together with power line carrier equipment and the system simulation also includes a very realistic non-linear fault arc model.

2. MODELLING OF THE SYSTEM

2.1 Power System

The series compensated EHV transmission line modelled in this simulation is based on a single circuit of the typical 500 kV horizontally constructed line application, the arrangement of which is as shown in Figure 1. The length of the line studied is 300 km, which is a double ended system of typical twin conductor with 20 GVA short circuit level capacity at the sending end and 0.5 GVA at the receiving end.

The transmission line is simulated by L.Marti's frequency dependent line model within the EMTP package. The system frequency used is 50 Hz. As regards the capacitor location, the most common system used in practice is the one employing a capacitor bank located close to each end of a line[2] and this is the system studied here. A typical level of compensation of 70% is used throughout.

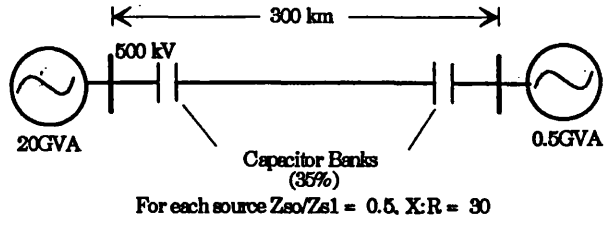

Figure.1: Single line diagram of the studied system

2.2 Capacitor Protective Schemes

In practice, there are a number of capacitor protective schemes in use. For moderate demands on capacitor reinsertion speed, protective spark gaps are still the most competitive solution. The dual gap scheme(DGS) of the type shown in Figure 2a and dual gap scheme with a non-linear resistor(DGNS) of the type shown in Figure 2b are very commonly employed. The latter has a number of distinct advantages over the former[5]. Modern series compensated systems also employ the MOV protective schemes(figure 2c) which provides a number of benefits including instantaneous reinsertion without transients, lower capacitor protective levels, greater reliability and lower maintenance[6,7]. The results presented here are for a DGS, DGNS and MOV.

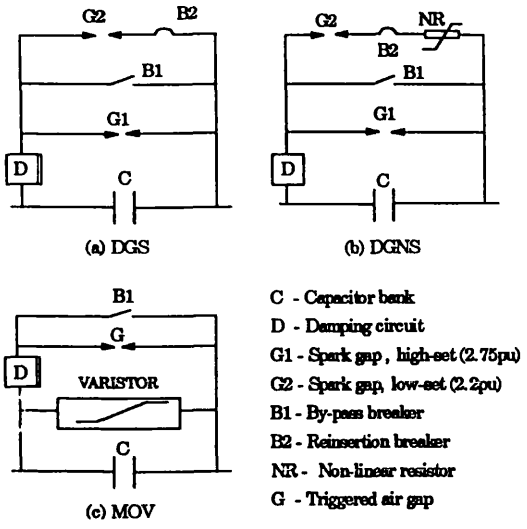

Figure. 2 Capacitor protective schemes studied

2.3 Stack Tuner and Line Trap Arrangement

Connected between the source and the outgoing transmission line at each terminal is the line trap and stack tuner arrangement. This is shown in Figure 3. The shunt busbar capacitance of $0.1\mu F$ is assumed at each terminating busbar.

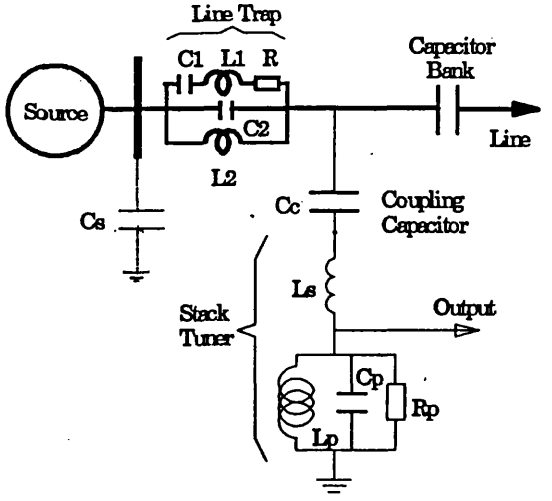

Figure.3 Stack tuner / line trap arrangement

The line trap is the standard type used in power line carrier applications and can be tuned to block a narrow band of high frequencies (i.e. offer a high impedance) whilst appearing to be a very low impedance at all other frequencies. Based on parameters obtained from the National Grid Company, the line traps were tuned to a centre frequency of 75 kHz.

The stack tuner is connected to the transmission line via the coupling capacitor of a standard CVT. It consists of a series tuning inductor Ls and a parallel RLC network tuned to the centre frequency of 75 kHz. The stack tuner is arranged so that it has a very high impedance at the power frequency (50 Hz) and is close to the line characteristic impedance at the tuned frequency (75 kHz).

The line trap / stack tuner arrangement shown in Figure 3 is connected to each of the three phases at both end of the series compensated line to be protected.

3. CHARACTERISTIC FEATURES OF THE MEASURED SIGNAL

Following a fault on the power system, the high frequency phenomena caused by the arcing and travelling waves propagate through the network at just below the speed of light. These wide-band fault generated high frequency noise signals can be captured using CVTs and conventionally connected power line carrier communication signal line traps. The high voltage capacitor of the CVT is used in conjunction with a specially designed stack tuner to capture the signals, whilst the line traps are used to confine the signals to the protected zone.
If the faults is internal to the line being protected, there will be a relatively consistent signal around 75 kHz from the output of stack tuner. If the fault is external then there will be severe attenuation of a very small band of high frequencies around the tuned frequency (75 kHz) due to the presence of the line trap and the busbar capacitance.

4. SIMULATION RESULTS

The digitally simulated test results have been studied at different fault inception angles of the pre-fault voltage and different fault points to represent both internal and external fault conditions. The results presented in this paper are only for single phase to earth faults (as these are the most common to occur) and the outputs shown are based on the stack tuner output responses corresponding to the faulted phase only.

4.1 Typical Internal and External Fault Studies with DGS and DGNS

Figures 4(i) and 4(ii) show the results for an internal voltage zero fault with DGS and DGNS respectively. First of all considering the period immediately following a fault (but prior to capacitor protective gap operations), the signals detected by the stack tuners, Figures 4(i)a & 4(ii)a, are identical and, as expected, the frequency spectra of the stack tuner outputs (Figures 4(i)c & 4(ii)c) show a fairly strong wide band of frequencies around 75 kHz. With regard to a fault external to the protected zone, the stack tuner outputs, (Figures 5(i)a & 5(ii)a) appear to be similar to the internal faults condition in the time domain. However, in the frequency domain, it can be clearly seen from Figures 5(i)c & 5(ii)c that the HF around 75 kHz are severely attenuated.

A comparison of the internal and external faults thus clearly shows that prior to gap flashover, the frequency spectra associated with the bursts of HF signals are similar to those generated on a plain feeder[3] and are little affected by the presence of the series capacitors.

4.2 Effect of Capacitor Gap Flashover

Figures 4d - 5d typify the frequency spectra of the stack tuner outputs, after capacitor gap flashover. It is apparent that in the case of a DGS, the additional bursts of HF noise (Figures 4(i)a, at T_2) generated on gap flashover are much higher in magnitude than the corresponding bursts associated with a DGNS (Figure 4(ii)a, at T_2); this is so by virtue of the fact that the step change associated with the former (Figure 4(i)b) is much larger than in the case of the latter (Figure 4(ii)b). The net effect of this phenomenon is that the frequency spectra in the case of DGS (Figure 4(i)d) is considerably modified, with little effect on the frequency spectra associated with the DGNS (Figure 4(ii)d). In the case of an external fault, similar observations can be made, as evident from Figures 5(i)d & 5(ii)d. Figures 6(i) & 6(ii) show the effect on the measured signal for an external fault occurring near voltage maximum with DGS and DGNS scheme respectively. Here it is apparent that, unlike the previous case of a voltage zero fault, the gap flashover has little effect on the frequency spectra of the HF signals.

4.3 Typical Internal and External Faults Studies with MOV Protective Scheme

Figure 7 shows the system response for both internal and external faults with MOV protective scheme for different fault-inception angles. In this case, the protection is independent of the action of any spark gaps and it is apparent that the conduction of the varistor has no effect on the frequency spectra of the HF signals.

5. CONCLUSIONS

This paper outlines a new technique for detecting the fault induced HF voltage signals in series compensated line. The simulation studies clearly show that the HF noise produced by capacitor spark gap operation can have a considerable effect on these signals generated, particularly if a DGS is employed. However, in the case of DGNS schemes, they are not adversely affected by the fault inception angle under both internal and external faults by the additional HF noise generated by the operation of the DGNS. For the MOV protective scheme, the results presented again demonstrate that frequency spectra of the HF signals are very distinctly different for both internal and external faults and they exhibit certain unique features which are unaffected by a whole variety of practical system and fault conditions. There is thus evidence to suggest that the new protection technique as developed for plain feeders is more suited to series compensated systems employing a DGNS and MOV.

Based on the accurate modelling and successful detection of the fault induced HF voltage signal, these signal can be employed to effect a new protection technique for series compensated lines and work in this area is now in progress at Bath.

6. ACKNOWLEDGEMENTS

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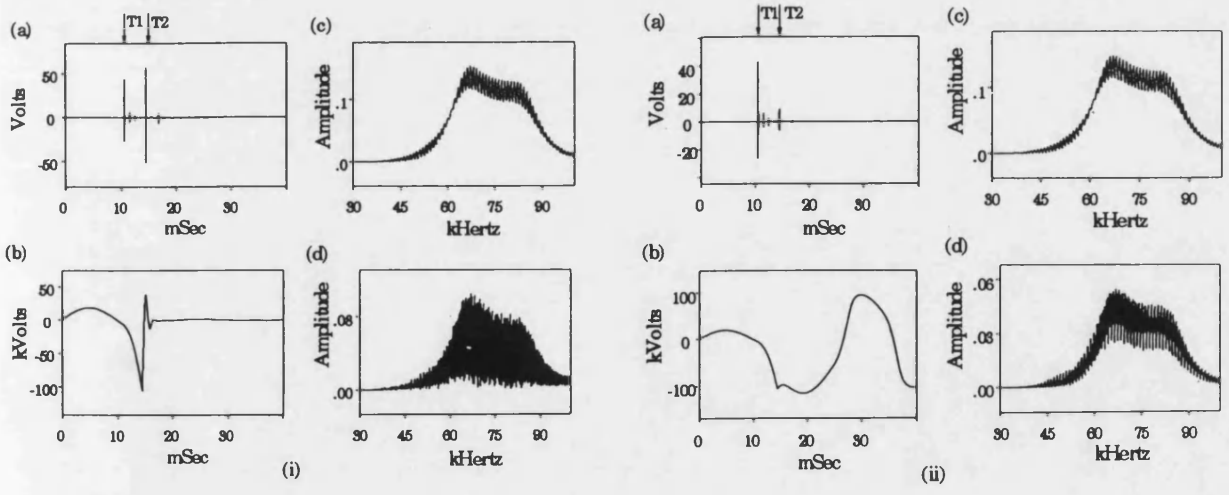

Figure 4: Typical response for a internal voltage zero fault

(a) Stack-tuner output
(b) Capacitor voltage waveform
(c) Spectra of stack-tuner output (before gap flashover)
(d) Spectra of stack-tuner output (after gap flashover)

(i) With DGS
(ii) With DGNS
T1 = fault inception
T2 = capacitor-gap flashover

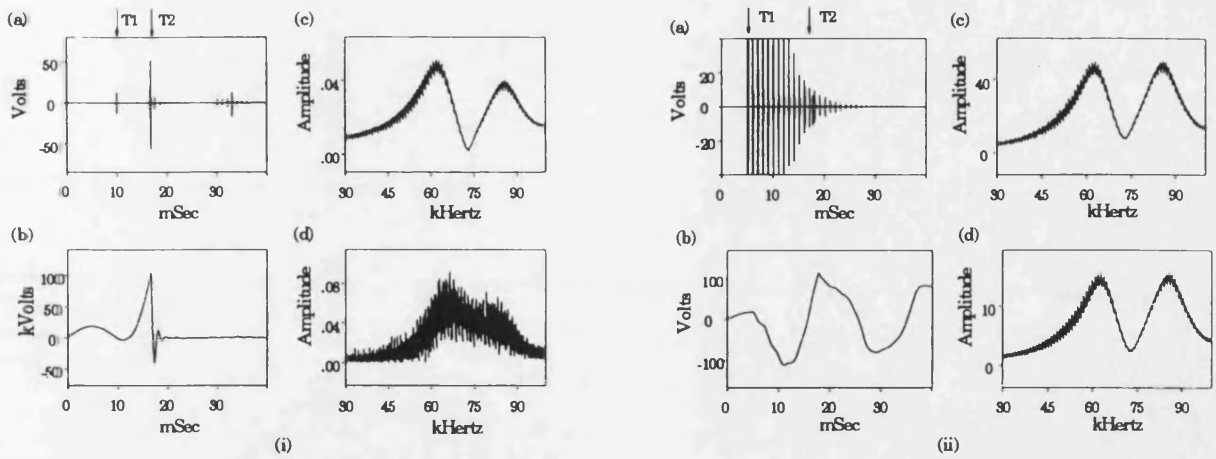

Figure 5: Typical response for an external voltage zero fault

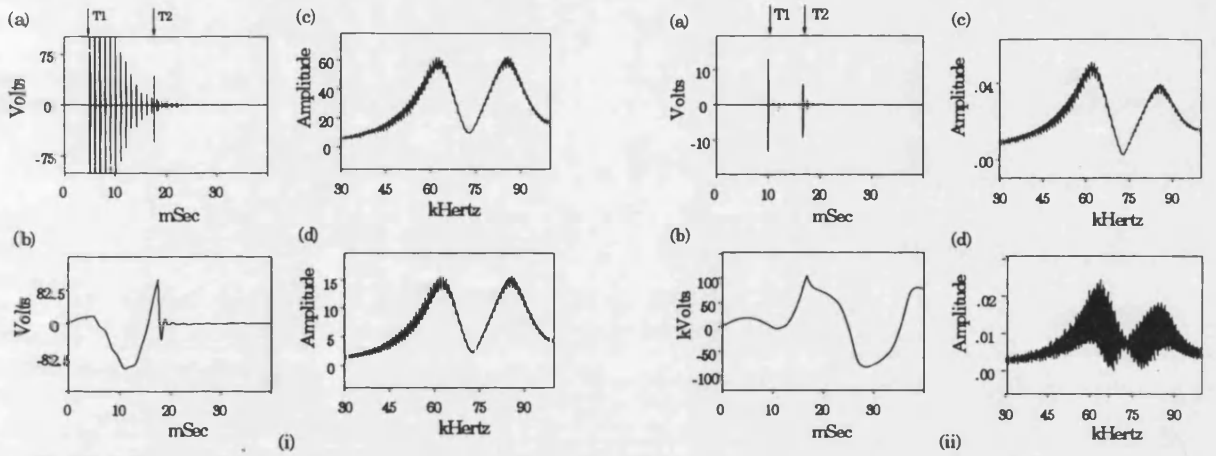

Figure 6: Typical response for an external voltage maximum fault

(a) Stack-tuner output
(b) Capacitor voltage waveform
(c) Spectra of stack-tuner output (before gap flashover)
(d) Spectra of stack-tuner output (after gap flashover)

(i) With DGS
(ii) With DGNS
T1 = fault inception
T2 = capacitor-gap flashover

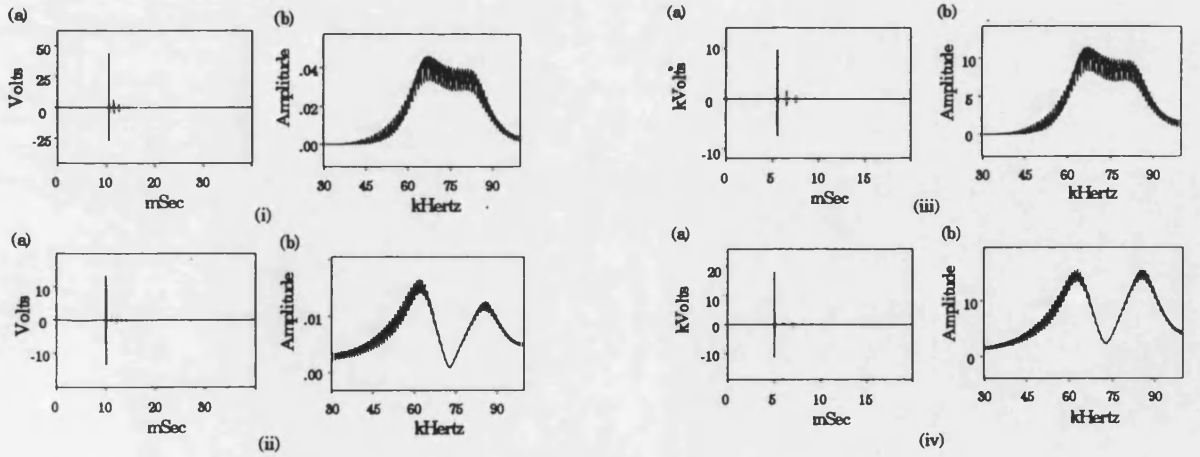

Figure 7: Typical response for a internal and external fault with MOV scheme

(i) Internal voltage zero fault
(ii) External voltage zero fault
(iii) Internal volatge maximum fault
(iv) External voltage maximum fault

(a) Stack-tuner output
(b) Spectra of stack-tuner

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A Novel Non-unit Protection for Series Compensated EHV Transmission Lines Based on Fault Generated High Frequency Voltage Signals

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Abstract: A new high-speed protection technique based on fault generated high frequency (HF) voltage signals is developed and applied to the protection of series compensated lines. It is a non-unit protection technique as it relies totally on locally derived information, but it has the discriminative properties normally associated with unit protection schemes. The protection scheme has been designed using computer-aided-design (CAD) techniques including emulation of analogue interface and hardware. It is shown that the new relay scheme is able to overcome many difficult protection problems encountered on such lines using conventional methods, and discriminates clearly between internal and external faults, producing a fast trip output.

Keywords: Transmission line protection, Series compensation, High-frequency signals, Arcing faults.

1. INTRODUCTION

Series capacitors are finding wide spread usage in EHV systems; essentially they help to: solve the problem of stability, increase power transmission capabilities, improve voltage control, etc. However, protection of systems with series compensated lines is considered to be one of the most difficult tasks for relay manufacturers and utility engineers [1]. For example, the distance relay reach measurement depends upon the status of the capacitor and the transient response of the capacitor protection circuit, the operation of which, in general, does not conform to any pre-defined pattern [2]. If a capacitor(s) is protected by a conventional single gap/dual gap scheme, the operation of the latter results into all the compensation being removed from the system; equally importantly, significant transient components (other than those generated by faults) can be impressed upon the voltage and current waveforms. On the other hand, if a capacitor is protected by a non-linear Metal-Oxide Varistor (MOV) element, there is always some compensation (which is variable) present in the system and the level present is dependent upon the location of the fault. Thus, due to the varying amount of capacitance in the circuit and additional transients being introduced, distance relays will have a tendency to maloperate.

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Other difficulties caused by the sudden removal and insertion of capacitors into the circuit are voltage and/or current inversion and loss of directionality in the case of directional line protection relays [3]. In this respect, some of the recently developed unit type protection schemes [4] based on a communication link between the two ends of the protected line, offer an adequate protection for long-distance series compensated lines. However, they require very reliable and expensive communication channels to avoid loss of integrity due to channel failure.

Line protection schemes, based on the monitoring of the non-power frequency components on overhead lines caused by a sudden change in the system voltage due to travelling waves and arcing faults etc, have been of interest for many years; this is so because they provide the possibility of obtaining very rapid fault clearance [5, 6]. However, these have been mainly confined to plain feeder applications and very little has been reported on their application to series compensated lines.

This paper describes a new protection technique for accurately detecting faults on series compensated lines; it is based on utilising the fault-induced HF signals at any one end of the line. The basic principles are essentially an extension of those reported in [7, 8] for plain feeders. The HF signals are captured using a specially designed stack tuner connected to a standard capacitor voltage transformer (CVT). Power line carrier (PLC) line traps are used to confine the HF signals to the protected zone and their bandstop characteristics are used as a basis for discriminating between internal and external faults. Consequently this is a non-unit protection technique as it relies entirely on locally derived information.

The main thrust of the work presented herein is to outline progress made in the design and development of a specially designed signal processing unit which is used to process the captured HF voltage signals. More importantly, it has been developed to satisfactorily deal with the aforementioned protection problems; it provides a performance which satisfies the requirements for reliable and secure protection of series compensated lines for a whole variety of practically encountered system and fault conditions. The performance of the designed relay is demonstrated by utilising fault data generated on practical 500kV long lines of the horizontal construction type. The transient fault studies are based on the well known Electromagnetic Transients Program (EMTP) software; the system simulation also includes a very realistic non-linear fault arc model together with models of different capacitor protective schemes.

2. BASIC PRINCIPLE OF THE PROTECTION SCHEME

The basic relay operating principle hinges upon detecting the fault generated HF voltage signals by using the stack tuner and line trap arrangement as shown in Fig. 1, which is connected to all three phases at each end of the transmission line being protected. The line trap and stack tuner are the standard type used in PLC applications and are the same as those described in [7]. They are tuned to a typical band 1 range of frequencies (70- 81kHz) with a centre frequency of 75kHz. Cs is the stray busbar capacitance, typically 0.1μF. It should be noted that in practice, the fault generated noise signals contain HF components over a wide bandwidth, with little attenuation of signals up to about 500kHz. This effectively means that within the constraints of the practical hardware available, particularly in terms of processing power and speed, the technique described herein can be equally applied over other frequency bands.

It has been shown in [9] that fault induced HF voltage signals in series compensated line can be successfully captured within two very distinct bands of frequencies. The basic relay principle thus depends on the formation of two discriminant signals using digital signal processing: an "operate" signal based on signal energy around the centre frequency and a "restraint" signal based on signal energy slightly off-centre frequency. The ratio of these two signals determines whether a fault is internal or external to the protected zone. For an internal fault, this ratio will be approximately equal to or greater than unity and for an external fault it will approach zero [7, 8]. Finally, this ratio activates a sophisticated decision process which comprises of a counter; it issues a trip decision when its value exceeds a predefined threshold level.

3. SYSTEMS STUDIED

A. Power system

There are a large number of possible capacitor locations and degrees of series compensation encountered in practice. However, the two most common systems are [1]: a capacitor

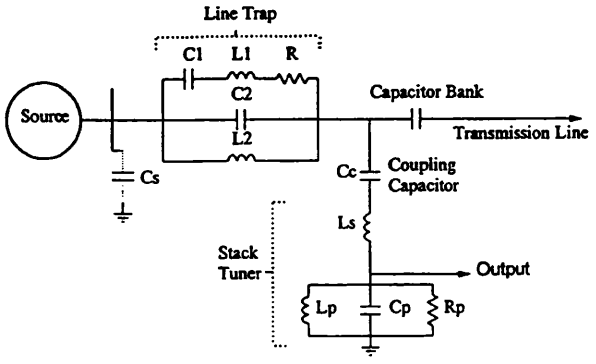

Fig. 1 Stack tuner / line trap arrangement

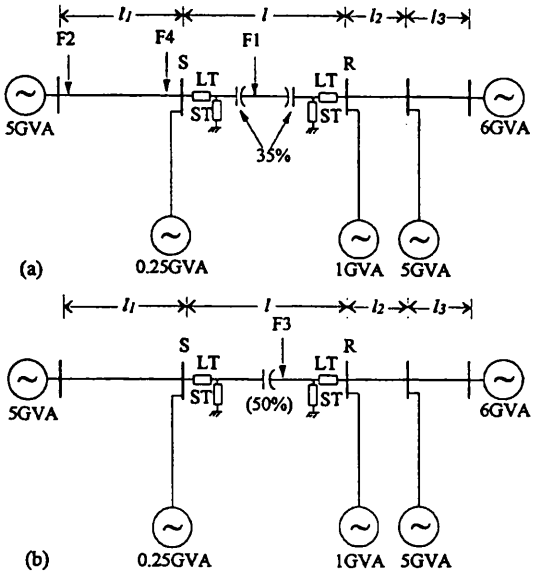

Fig. 2 Typical system configurations studied
All 500 kV lines of lengths *l1 = l = 300 km, l2 = l3 = 150 km*;
For each source Zso/Zs1 = 0.5, X:R = 30; ST = stack tuner, LT = line trap
(a) compensation at the line ends (b) compensation at the midpoint

bank located in the vicinity of each line end and a single capacitor bank located at the middle of the line. The relay performance has been evaluated using the universally accepted EMTP software for the two aforementioned network configurations shown in Figs 2a and 2b. In the case of the former, a typical level of compensation of 70% is used, whereas in the case of the latter 50% compensation is assumed. The results presented here relate to a typical single-circuit 500kV horizontally constructed line commonly employed in long distance transmission applications in many overseas countries. The frequency dependence of the line parameters has been taken into account, a system frequency of 50Hz is used and an earth resistivity of 100Ωm is assumed. A realistic primary arc model, as has been developed in [10], is embodied into the system simulation to represent the nonlinear behaviour of the fault arc path.

B. Capacitor Protective Schemes

Series capacitor compensation is economically feasible when auxiliary devices are used to protect the capacitors against overvoltages during system faults. In practice, there are a number of capacitor protective schemes in use. The traditional gap-type scheme has been extensively used for series capacitor protection against overvoltages [2, 11]. The conventional dual gap scheme (DGS) of the type shown in Fig. 3a and the dual gap scheme with a non-linear resistor (DGNS) of the type shown in Fig. 3b are commonly employed. When an excessive current flows, the protection ensures that this current is diverted through the spark-gap, thereby partially or completely removing the compensation from the circuit, depending on the design of the by-pass circuit. Modern series compensated

systems also employ the MOV protective scheme (Fig. 3c) which provides a number of distinct advantages over the former two, including instantaneous reinsertion without transients, lower capacitor protective levels, greater reliability and lower maintenance [12]. Since they are likely to find more widespread usage, it is important to understand the basic principles (including mathematical modelling) of a MOV; these have been summarised in the Appendix.

Although the results presented are mainly for a system employing a MOV, some results are also given in order to demonstrate the satisfactory performance of the relay technique developed herein for systems employing the capacitor protective schemes of the types shown in Figs. 3a and 3b. For the systems considered, the voltage level associated with a 1p.u. gap setting has been taken to correspond to a typical line loading of approximately 1GVA. For example, for 70% compensation with a capacitor bank near each line end, a 2.2 p.u. gap setting (this is the setting employed in this study) would correspond to a capacitor sparkover voltage of 114 kV peak.

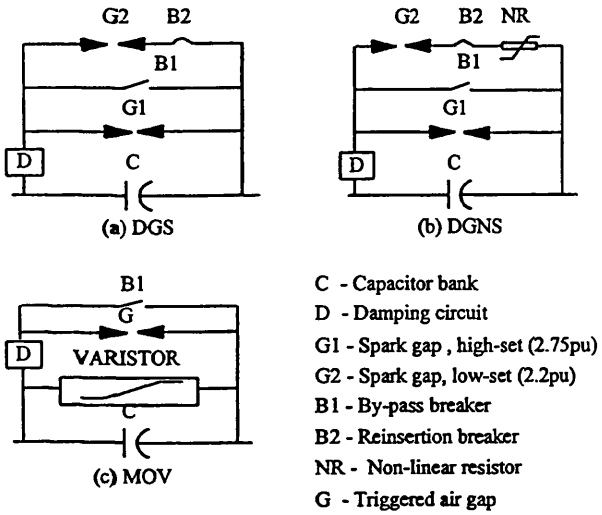

Fig. 3 Capacitor protective schemes studied

4. RELAY STRUCTURE

A. Overview

Fig. 4 shows a block schematic diagram of the complete protection scheme which comprises of analogue and digital parts. The design of the former is essentially the same as that outlined in reference [8]. Briefly, the output of each stack tuner (V_a,V_b,V_c) is combined to form modal signals of the form [mode-2 = V_a-2V_b+V_c] and [mode-3 = V_a-V_c] in such a manner as to cover all types of fault encountered in practice. With these combinations, any common-mode signals (due to mutual coupling) induced in the line which result, for example, from adjacent parallel lines and/or multiple circuits sharing the same right of way are eliminated; this ensures immunity to all disturbances other than those associated with the line to which the protection equipment is connected. This would also be true in the case when parallel lines have line traps tuned to different centre frequencies. It should be noted that the technique can equally be applied to the phase voltages V_a, V_b and V_c directly rather than transforming them to modal signals; However, in this case there is a high possibility of relay instability under external faults due to the aforemention reasons.

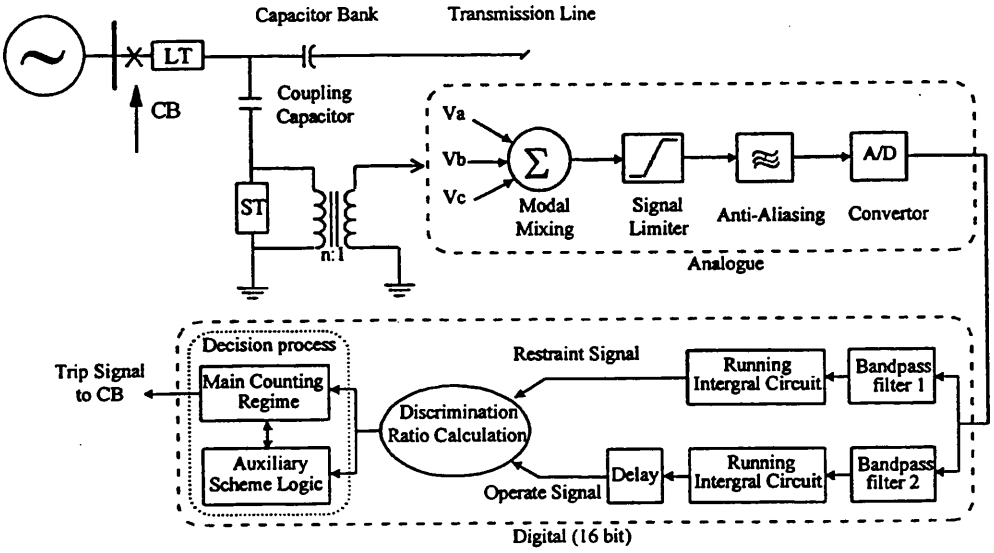

Fig. 4 Block schematic diagram of complete protection scheme
LT = line trap, ST = stack tuner, CB = circuit breaker

The modal signals are then passed through a limiter before being digitised through a 16-bit A/D converter. In this respect, it should be mentioned that although the latter gives a high resolution, some signal limitation is necessary in order to cope with the large dynamic range associated with fault generated HF signals. The outputs from the stack tuners are thus first stepped down by an auxiliary transformer. In practice, this comprises of a specially designed low-loss core which has a very wide bandwidth capable of passing HF frequency components with little attenuation. The turns ratio of the auxiliary transformer is carefully chosen to ensure coverage of a wide dynamic range necessary to cater for a majority of practically encountered fault generated HF signals. The attenuated signals from the transformer are limited to ±10V and are passed through a 2nd-order Butterworth filter with a cutoff frequency of approximately half the digital sampling frequency of 200 kHz; this is to avoid any errors arising through signal aliasing. In order to prevent the relay responding to any spurious system noise, a minimum threshold level of 20mV (this corresponds to a digital level of 65 quanta for the ±10V 16-bit A/D converter) is incorporated within the relay algorithm; this level corresponds to practical standing-noise levels typically encountered in a high voltage environment.

B. Digital Signal Processing

The digital part comprise digital filters, running integral circuits and a decision process. The A/D outputs are fed to two parallel connected digital narrow bandpass filters which are tuned to different centre frequencies. Sixth order elliptic infinite impulse response (IIR) filters are used as they give a very rapid transition between stop and pass bands, with a minimum filter order, and therefore, minimum group delay: the Z-plane transfer functions of this filter is given as:

$$H(Z) = \prod_{k=1}^{3} \frac{a_{0k}+a_{1k}Z^{-1}+a_{2k}Z^{-2}}{1+b_{1k}Z^{-1}+b_{2k}Z^{-2}} \qquad (1)$$

where a_{nk} and b_{nk} are the filter coefficients.

The operate filter frequency is fixed by the centre frequency of line trap, in this case 75kHz. The restraint filter frequency is chosen through an extensive series of studies for optimal relay performance. These studies involved examining the small drifts in the tuned centre frequency of the line trap resulting from a variation in the stray busbar capacitance Cs and/or small drifts in the line trap parameters caused by environmental factors. For the application considered here, a 2kHz bandwidth filter was used at the operate centre frequency of 75kHz and a 1kHz bandwidth filter at the restraint centre frequency of 60kHz. The outputs of the bandpass filters are then used to evaluate a running integral over a 1.25ms (250 samples) window. This gives a measure of the spectral energy content of the signals and results into the formation of enhanced "operate" and "restraint" signals. Because the IIR filters have slightly different group delays, the "operate" signal has to be delayed, in this case by 40 samples. The discrimination ratio is calculated by dividing the "operate" signal by the "restraint" signal. For internal faults, this ratio will be greater than unity, whereas it will be very close to zero for external faults; the latter is so by virtue of the fact that for an external fault, there is heavy attenuation of of the signal level at the centre frequency of 75kHz (this is the operate signal).

C. Decision Process

A specially designed decision process has also been incorporated into the relay algorithm to improve the relay security. It comprises a counter whose value is incremented or decremented according to the value of discrimination ratio, and is summarised in Table 1. As can be seen, when the discrimination ratio (*d*) is close to or above unity, the counter is incremented rapidly as the ratio gives a strong indication of an internal fault, whereas the counter is decremented rapidly when the ratio is close to zero as this gives a strong indication of an external fault. However, its values is never allowed to fall below zero.

Table 1. The decision logic

Discrimination ratio,*d*	Counter increment
$d \geq 1.0$	+10
$1.0 > d \geq 0.8$	+8
$0.8 > d \geq 0.6$	+4
$0.6 > d \geq 0.4$	+1
$0.4 > d \geq 0.2$	-1
$0.2 > d \geq 0.1$	-4
$0.1 > d \geq 0.01$	-8
$0.01 > d$	-10

It should be noted that, unlike with plain feeders, in series compensated lines there can be present some spurious HF noise in the relaying signals, in addition to the noise generated by genuine arcing faults, and this is as a direct result of the operation of the capacitor protective gaps, which (as mentioned before) is very random in nature. Whilst this is of no consequence for internal faults since any additional HF noise arising from capacitor gap flashover actually enhances relay performance by augmenting the signals, it can threaten relay stability of a healthy circuit for an external fault. Thus apart from the aforementioned counting regime, there is a concomitant requirement to build into the decision process an auxiliary scheme logic. In this respect, an extensive series of

studies have revealed that there is always a significant time lapse ($\geq$ 5ms) between the occurrence of an external fault and any gap flashover on a healthy circuit. In the relay scheme described herein, the problem of possible relay instability has thus been overcome by simply monitoring the behaviour of the decision counter in a small window length w_p following a fault; if it stays well below the trip level over the entire period associated with this window, the fault is assumed to be external and the counter is simply set to zero and not allowed to increase thereafter.

Extensive CAD studies were carried out to ascertain the optimum settings of the decision process and trip level. For the relay described here, the above mentioned fixed window length w_p set to 600 samples (3ms) and a trip level of 100 have been found to give a rapid relay trip for internal faults whilst the counter remains well below this level and restraints for external faults. A decision process of this nature thus provides a near optimum performance in which the relay retains its maximum sensitivity in the initial fault detection period (particularly for internal faults) and any relay mal-operation is prevented from occurring for the external fault during the entire period that the signals become significantly finite after capacitor gap(s) flashover. It should be mentioned that the auxiliary scheme logic based on a window length w_p=3ms has no detrimental effect on relay performance for internal faults.

5. RELAY RESPONSE EVALUATION

The performance of the new protective relay was evaluated for the two network configurations shown in Figs. 2a and 2b, for different capacitor protective schemes and some of the results have been discussed below. It should be mention that due to a limitation of space, only the performance associated with aerial mode-2 signals is shown. The performance attained using aerial mode-3 signals for the faults is not presented here.

A. Relay performance for internal faults

Fig. 5 typifies the relay performance for an 'a'-phase to earth fault with the MOV capacitor protective scheme. The fault is applied when the a-phase voltage is passing through 30°, and the fault is at 80km from end S on the line *l* of the network shown in Fig. 2a, at F1. The behaviour of the MOV for this fault condition is illustrated in Figs. 5a and 5b; as expected, both the capacitor current and voltage increase on fault inception. Once the capacitor voltage rises above a certain level, the MOV conducts and limits further voltage increase; this voltage is limited on each half cycle and the current alternates between the capacitor and the varistor. The capacitor/MOV shared conduction continues until the fault is cleared by the opening of the main line circuit breakers. The time domain responses of the composite signals at end S and end R as captured by the stack tuners are shown in Figs. 5c and 5e respectively. Figs. 5d and 5f show their corresponding frequency spectra. The first noise burst arrives a short time

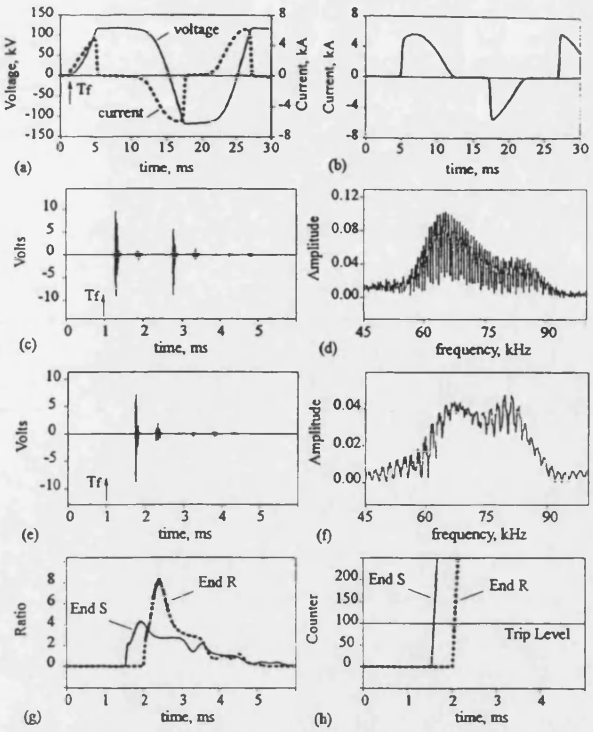

Fig. 5 Relay response for an internal a-e fault at F1 in Fig. 2a: with MOV scheme
Tf = fault inception time
(a) End S a-phase capacitor waveforms (b) End S MOV / bypass current
(c) End S composite signal (d) End S spectra of composite signal
(e) End R composite signal (f) End R spectra of composite signal
(g) Discrimination ratios (h) Counter outputs

after fault inception because of the time taken for the signals to propagate along the transmission line from the fault point. The successive bursts are due to a combination of HF components generated by the non-linear behaviour of the primary arc and travelling wave components. These arise due to reflections from the impedance discontinuities in the circuit such as at the fault point and the line ends. In the frequency domain (Figs. 5d, 5f), the signal strengths at the two filter centre frequencies (i.e 60 kHz and 75 kHz respectively) are comparable and this is confirmed by the discrimination ratios (Fig. 5g) which are well above the requisite level of 'one'. When considering the function of the decision process, Fig. 5h clearly shows that for this internal fault, the decision counters quickly attain the required trip level and issue the trip decisions in approximately 0.6ms and 1ms after fault inception at ends S and R, respectively. The additional delay associated with the end R relay is as a direct consequence of the transit times involved in the HF components travelling from the fault point to end R. It should be mentioned that these tripping times do not take into account any delays due, for example, to the data processing times, the numeric calculation times within the floating point processor, etc. In practice these are likely to add a few milliseconds to the overall relay operating times; more importantly, the latter will still be < 5ms in a practical implementation of the technique.

B. Relay performance for external faults

Fig. 6 typifies the relay performance for a remote-end 'b'-'c' phase fault behind the relay at end S (at F2 in Fig. 2a), again for a system employing MOV capacitor protective schemes; the fault occurs when the 'a' phase voltage is passing through zero. The time domain responses of the composite signals at ends S and R (Figs. 6a and 6c) appear to be very similar to the internal fault case. However, in the frequency domain, the blocking effect on the narrow band of frequencies around 75kHz can be clearly seen from Figs. 6b and 6d. At both line ends, the discrimination ratio peaks at approximately 0.1 (Fig. 6e), and as this is well below unity, the counter outputs remain at zero and hence no trip decisions are asserted (Fig. 6f).

C. Relay performance for conventional gap-type capacitor protective schemes

Fig. 7 depicts the performance of the relay at end S following an 'a'-'b'-earth internal fault, at the mid-point of the line *l* for the arrangement shown in Fig. 2b, at point F3, with DGS and DGNS respectively. The fault occurs when the 'a' phase voltage is going through -30°. In the case of the DGS, this particular fault condition results in phases 'b' and 'a' capacitor gap flashovers in approximately 5ms and 6.5ms after fault, respectively, whereas in the case of DGNS only the phase 'b' capacitor gap flashes over, as evident from Figs. 7a and 7b.

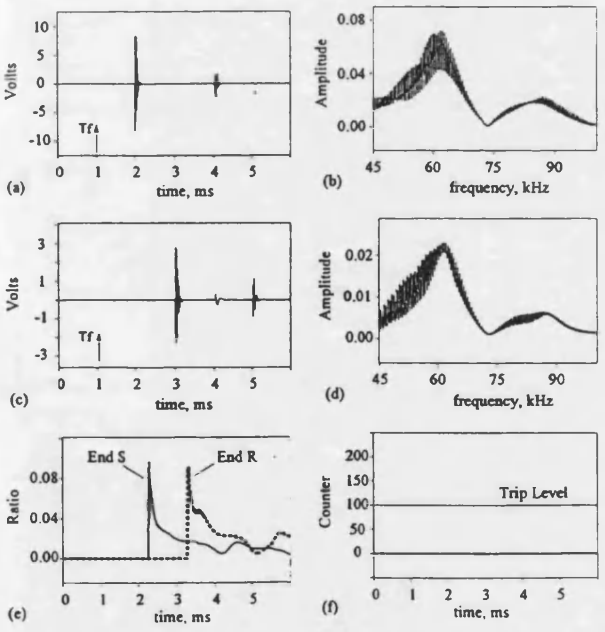

Fig. 6 Relay response for an external b-c phase fault at F2 in Fig. 2a: with MOV scheme; Tf = fault inception time
(a) End S composite signal (b) End S spectra of composite signal
(c) End R composite signal (d) End R spectra of composite signal
(e) Discrimination ratios (f) Counter outputs

Comparing the capacitor voltage waveforms, it can be seen that the DGS causes the capacitor voltages to be clamped down to almost zero after gap flashover. The DGNS, on the other and, adequately protects the capacitor against overvoltages (by limiting the latter), whilst maintaining a substantial voltage across it (Fig. 7b); this can be directly attributed to the characteristic of the non-linear resistor.

When considering the relay measurands, Fig. 7c and 7d show that the time domain responses of the composite signals at end S for both DGS and DGNS are almost identical and the relay response is very similar for both cases as shown in Figs. 7e, 7f and 7g; the relay asserts a trip decision in approximately 1ms after fault inception. It should be noted that although not shown here, the end R relay performance is almost identical to that at end S for this fault condition.

As mentioned before, in series compensated systems, a potential problem exists in situations where a high level fault external to the protected line causes capacitor protection gap(s) to flashover; this in turn, causes a disturbance which can appear to be internal to the protected line. Thus, it is vitally important to verify that the relay performance is satisfactory under such situations.

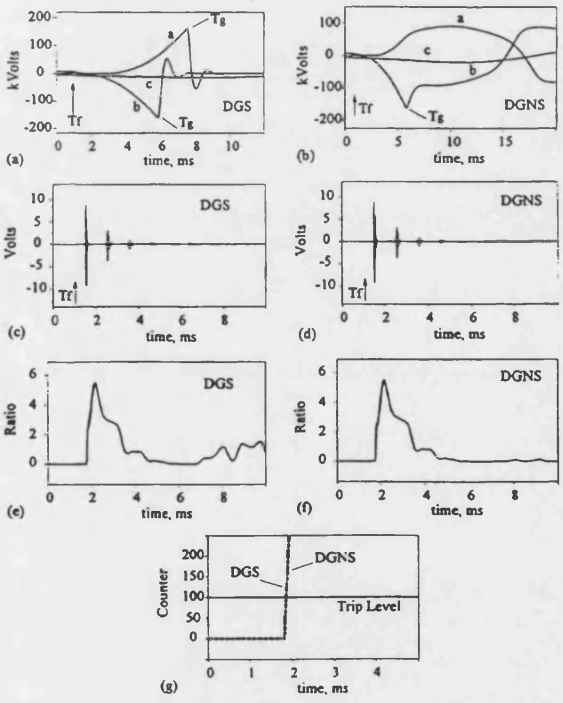

Fig. 7 Relay performance for conventional gap-type schemes:
Internal a-b-earth fault at F3 in Fig. 2b
Tf = fault inception time Tg = capacitor-gap flash over
(a), (b) End S capacitor voltage waveforms (c), (d) End S composite signals
(e), (f) Discrimination ratios at End S relay (g) End S relay counter outputs

Fig. 8 shows the relay response to an 'a'-earth external fault near voltage zero of the 'a' phase voltage, immediately behind the line trap and on the busbar at the end S (at F4 at Fig. 2a). In this particular fault study, the 'a' phase capacitor gaps at end S flashover in approximately 7ms after fault for both DGS and DGNS (see Figs. 8a,8b). Considering the time domain response of the composite signal at end S, it is evident from Figs. 8c and 8d that in the case of a DGS, the additional bursts of HF noise generated on gap flashover are much higher in magnitude than the corresponding bursts associated with a DGNS, and can be directly attributed to the relatively large voltage step change associated with the former on gap flashover. The net effect of this phenomenon is that the discrimination ratio in the case of the DGS rises above 'one' after gap flashover (i.e 7ms after fault inception), but stays significantly below unity in the case of the DGNS. More importantly, the discrimination ratio stays well below unity for a significant time period after fault inception and as a consequence, the auxiliary scheme logic within the decision process (as described previously) recognises this as an external fault and inhibits any increment in the counter output once the pre-defined time window of 3ms has been surpassed; this is evident from Figs. 9g and 9h. It is important to note that this potential problem due to gap flashover is only endemic in systems employing DGS capacitor protective scheme.

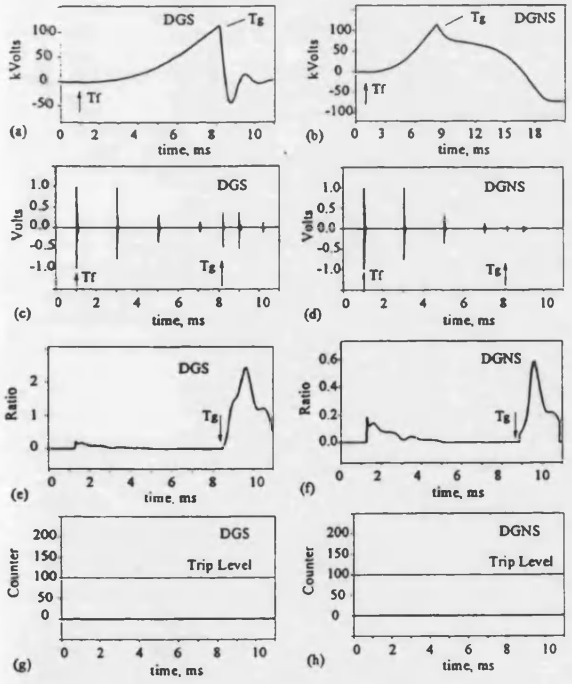

Fig. 8 Relay performance for conventional gap-type schemes:
External a-earth voltage-zero fault at F4 in Fig. 2a
Tf = fault inception time Tg = capacitor-gap flash over
(a), (b) End S a-phase capacitor voltage waveform
(c), (d) End S composite signals (e), (f) Discrimination ratios at End S relay
(g), (h) End S relay counter outputs

Fig. 9 shows an example of the relay performance for the same 'a'-earth external fault, ie. at point F4 on the network shown in Fig. 2a, but this time the fault inception angle is near 90^0. In marked contrast to the previous case of the voltage zero fault, the bursts of the HF signals generated by a genuine arcing fault (augmented by a significant travelling wave component) are much larger in magnitude in comparison to the additional HF components generated on gap flashover, which occurs approximately 8ms after fault inception. As expected, for this external fault, the discrimination ratios remain well below unity (< 0.2) and as a consequence, the relays remain stable for both DGS and DGNS, as evident from Figs. 9g and 9h.

D. Relay performance under non-arcing faults

In practice, although over 90% of faults in power transmission systems are arcing faults, other types of faults do occur, for example non-arcing permanent faults, involving high resistance. It is thus important to test the new relay scheme for such faults. Fig. 10 shows the relay response for an 'a'-phase to earth non-arcing fault involving fault resistance of 25Ω and 250Ω. The faults are applied when the 'a'-phase voltage is passing through 10^0, and the fault is at 80km from the end S, at F1 in Fig 2a; again MOV scheme is employed. As expected,

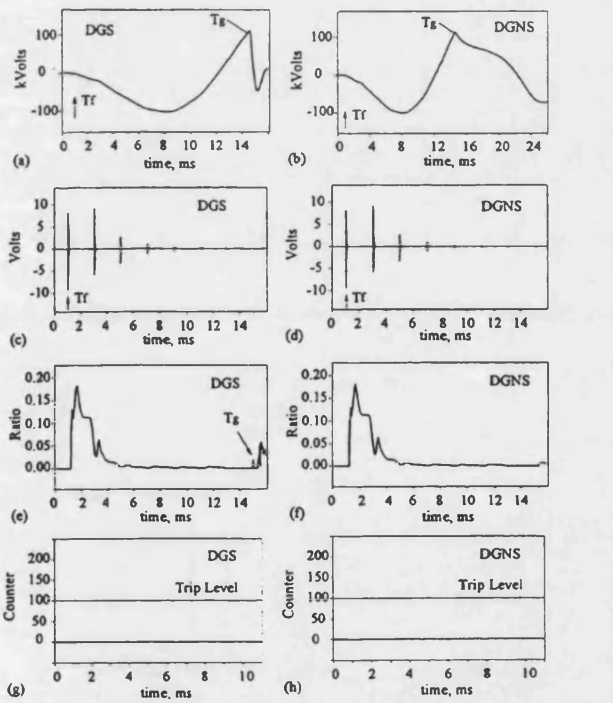

Fig. 9 Relay performance for conventional gap-type schemes:
External a-earth voltage-maximum fault at F4 in Fig. 2a
Tf = fault inception time Tg = capacitor-gap flash over
(a), (b) End S a-phase capacitor voltage waveform
(c), (d) End S composite signals (e), (f) Discrimination ratios at End S relay
(g), (h) End S relay counter outputs

although the magnitudes of the HF signals are attenuated by the increase in the fault resistance (see Figs. 10a and 10b), the ratio between the operate and restraint signal is unchanged and hence this has little bearing on the performance of the protective relay, as clearly evident from the relay performance shown in Figs. 10c-10f. It should be noted that in the absence of fault arcs, the HF phenomenon is due to the travelling wave effect. A series of CAD studies has shown that, although the relay can theoretically detect faults involving resistances well above 500Ω, in practice the upper limit of tolerance is likely to depend heavily on the levels of spurious noise induced in the electronic circuitry in the hostile environment of a substation.

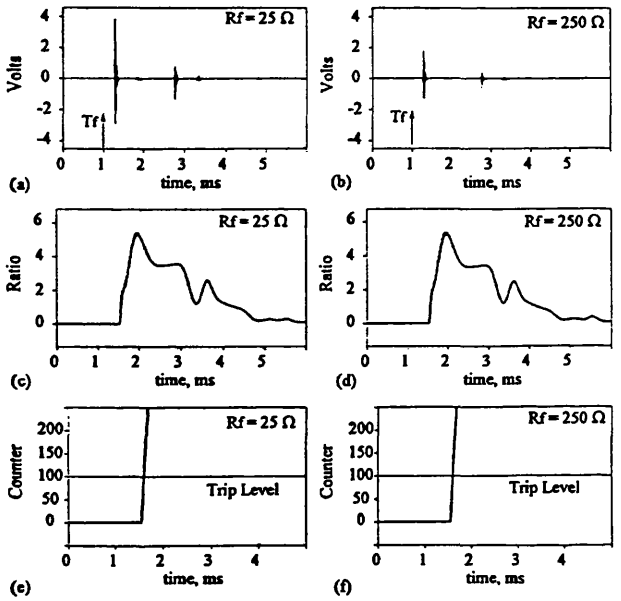

Fig. 10 Relay performance under non-arcing faults:
Tf = fault inception time Rf = fault resistance
(a), (b) End S composite signals
(c), (d) Discrimination ratios at End S relay
(e), (f) End S relay counter outputs

6. CONCLUSIONS

This paper describes the design and performance of a new protection scheme based on the detection of fault generated HF signals under arcing faults, as applied to EHV series compensated systems. The scheme possesses unit-protection discriminative properties without the need for a communications channel linking the protection at each end of a line. It thus eliminates any loss of integrity which might otherwise arise as a result of communications channel failure. The fault generated HF signals are captured from the system by means of a specially designed stack tuner and the high voltage capacitor of a conventional CVT, and fed into a digital signal processing unit. The relay algorithm developed, including the special decision process, enables the scheme to give correct performance under all types of practically encountered fault, both internal and external. The results presented clearly show that the relay maintains its dependability and security for systems employing different types of capacitor protective scheme and is virtually immune to changes in compensation/additional transients emanating from the operation of such schemes under faults. This is a significant advantage over conventional line protection relays.

This new protective technique based on non-unit principle, signifies an important breakthrough in the protection of series compensated lines which, although highly attractive both from an economic and environmental points of view, hitherto have found limited applications in view of less than satisfactory performance being possible with conventional non-unit protection techniques. It should be mentioned that although the technique described herein is designed for transmission systems employing power line carrier equipment comprising specialized line trap/stack tuner units and can therefore involve additional costs, the alternative for satisfactory protection of series compensated lines would be unit-type protection based on expensive communication links. It should also noted this technique works equally well on a transmission system with plain feeders as outlined in refs. [7, 8]. Finally, although the technique presented here is suited to systems employing three phase tripping; work is now in progress at the University of Bath [13] to extend the principle to systems employing single pole applications which require an accurate selection of the faulted phase.

7. ACKNOWLEDGMENTS

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9. APPENDIX

A. Simulation of the MOV capacitor protection scheme

If the volt ampere characteristic of a particular MOV-based protection is known, an elaborate multi-exponential zinc oxide model is available within the EMTP software to accurately reproduce this data. A typical circuit configuration of a MOV-protected series capacitor is shown in Fig. 3c and its nonlinear volt- ampere characteristic can be given in analytical form as:

$$I = \left[\frac{V}{V_N}\right]^n$$

V_N is a characteristic voltage of the arrestor which defines the proportionality between I and V^n; the value of n is typically chosen from 30 to 50. To determine V_N, I_{max} (peak) is substituted for I and V_{pk} for V:

where

V_{pk} - protective (peak) voltage level of MOV

$V_{pk} = \sqrt{2} I_{pr} X_c$

X_c - reactance of the capacitor

I_{pr} - protective current level of MOV (typically 2.5 times the rated capacitor bank current)

If I_{max} is unknown, an assumed value of 15 - 20kA can be used.

The MOV is designed to operate randomly according to different fault conditions and to hold the capacitor voltage at or below the value of V_{pk} even for the largest available system current I_{max}.

10. BIOGRAPHIES

J.A.S.B. Jayasinghe was born in Sri Lanka in 1965. He received the B.Sc. (Eng.) degree with First Class Honours in Electrical and Electronic Engineering from the University of Peradeniya, Sri Lanka. He joined the same university as a lecturer in 1993. He is presently studying in the School of Electronic and Electrical Engineering, University of Bath for his PhD. His current research interests include Digital Protection and Power System modelling and simulation.

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